Present and Future Needs of Free-Space Optical Interconnects

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Abstract. Over the last decade significant progress in optoelectronic devices and their integration techniques have made Free-Space Optical Interconnects (FSOI) one of the few physical approaches that can potentially address the increasingly complex communication requirements at the board-to-board and chip-to-chip levels. In this paper, we review the recent advances made and discuss future research directions needed to bring FSOI to the realm of practice.
Keywords: Optical Interconnects, Optical Packaging, Micro-optics, OptoElectronics, Free-Space Optical Interconnects

1 Introduction

Exchanging data at high speed over sufficiently long distances is becoming a bottleneck in high performance electronic processing systems [1,2,3]. New physical approaches to dense and high-speed interconnections are needed at various levels of a system interconnection hierarchy starting from the longest interconnections: board to board, MCM to MCM on a board, chip-to-chip on a multi-chip module (MCM), and on-chip. For the next decade, FSOI when combined with electronics offer a potential solution [4,5,6,7,8,9] at the inter and intra-MCM level interconnects promising large interconnection density, high distance-bandwidth product, low power dissipation, and superior crosstalk performance at high-speeds [10,11,12,13].

2 Present Status of FSOI

Opto-Electronic (OE) devices including Vertical Cavity Surface Emitting Lasers (VCSELs), light modulators, and detectors have now been developed to a point that they can enable high speed and high-density FSOI [14,15,16]. Flip-chip bonding offers a convenient approach to their integration with silicon. For example, members of the 3-D OESP consortium (Honeywell Technology Center and University of California, Santa Barbara) have demonstrated FSOI links operating up to 2.5Gb/s between VCSEL arrays and suitable detector arrays. These developments occurred at an opportune time when high performance workstation manufacturers struggle to resolve communication bottlenecks at the board-to-board level. As a result, high efficiency FSOI links between VCSEL and detector arrays has sparkled the interest of

high performance workstation manufacturers such as Sun Microsystems. While board-to-board interconnect solutions using FSOI are now being evaluated by the computer industry, chip-to-chip interconnects are being investigated at a more fundamental level at several universities including UCSD. One of the key issues that needs to be addressed at this level is packaging. Indeed a packaging architecture and associated technologies need to be developed to integrate OE devices and optical components in a way that is fully compatible with conventional electronic multi-chip packages.

Recently at UCSD, we developed and demonstrated the operation of a fully packaged FSOI system for multi-chip interconnections capable of sustaining channel data rates as high as 800Mb/s. A picture of this system is shown in Figure 1. A conventional PCB/ceramic board is populated with silicon and OE chips and mated to a FSOI layer that is assembled separately. Design considerations, packaging approaches as well as testing results indicate that it is now possible to build FSOI electronic systems that are compatible in packaging techniques, physical dimensions and used materials with conventional electronics.

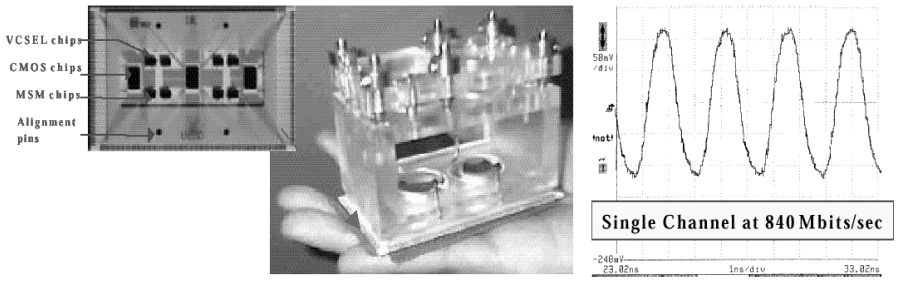

Figure 1. Fully packaged FSOI system

The overall packaging approach consists of the assembly of two different packaging modules: the opto-electronic module (multi-chip carrier and the OE chips (VCSEL, MSM and silicon chips), and the optics (FSOI) module. In our approach both modules are assembled separately then snaped on together. A mechanical pin-pinhole technique combined with alignment marks makes the alignment of the two modules a rather straightforward task. The optics module is built out of plastic except for the glass optical lenses that were commercially available. In the current demonstration system, four one-dimensional (1D) proton implanted VCSEL arrays (1´12 elements each) and four 1D Metal-Semiconductor-Metal (MSM) detector arrays (1´12) are used as light sources and photodetectors, respectively. The lasers and detectors are on a 250μm pitch. The VCSELs operate at 850nm with 15o-divergence angle (full angle at $1/e^2$), and the detector aperture is 80´80μm. Laser drivers, receiver (amplifiers), and router circuits are integrated on three silicon chips and included into the system. VCSEL arrays are optically connected to their corresponding detector arrays. Data can be fed electrically to any one of the silicon chips and routed to the VCSELs through driver circuits. The silicon chips also contain receiver circuits directly connected to the detectors; thus, data can also be readout electrically from each silicon chip independently.

In this FSOI demo system, 48 optical channels each operating up to 800Mb/s with optical efficiencies exceeding 90% and inter-channel crosstalk less than -20dB were implemented in a package that occupied less than 5x5x7 cm3. All channels were operational. This packaging technique is now being applied to demonstrate an FSOI connected board that is populated by three 3-D stacks of silicon chips. Each stack contains 16 silicon chips each hosting a 16x16 crossbar switch. In addition each stack is flip-chip bonded to a 16x16 array of VCSELs and detectors and communicates with other stacks via these devices. Thus with this package of very small footprint, 48 silicon chips will be interconnected via FSOI with each other.

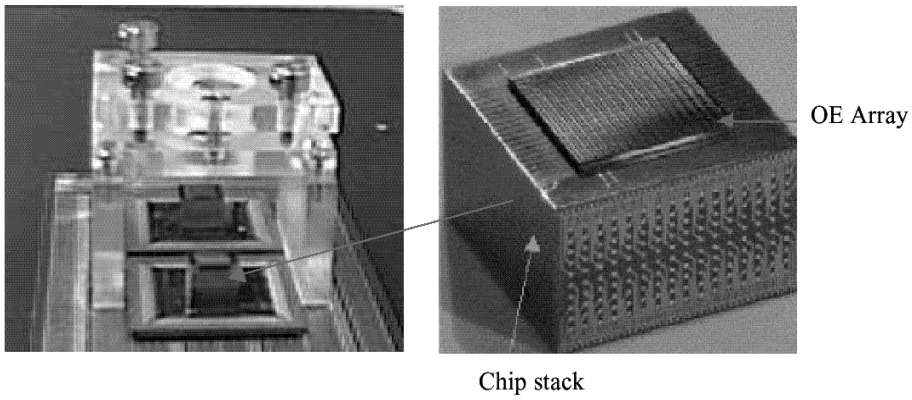

Figure 2. Application of UCSD's chip-to-chip FSOI packaging technique to 3-D stack-to-stack communication

3 Present limitations in FSOI and future directions

Although the demonstrations described above are important milestones in the quest for using optics within the board, it also underlines some of the present limitations of FSOI. These shortcomings include the:

- height of the optical package
- signal integrity and synchronization issues
- thermal stability of the assembly
- effective CAD tools
- ultra low voltage light modulation
- costs associated with FSOI.

To reduce the height of the package micro-optical elements compatible with oxide confined VCSELs need to be developed and become commercially available. Presently commercially available micro-optical components do not provide simultaneously the necessary high efficiency, low F# and spatial uniformity. In addition, communication within the box requires very low bit error rates. It is therefore critical to use extensive encoding techniques to minimize the error rates in FSOI. To this end there is a need for more silicon real estate and power consumption.

As the power in the package is increased passive alignment techniques may not be sufficient. Active alignment techniques based for example on MEMs components or special alignment facilitating OE Array Chip stack OE Array.

Chip stack.optical components must be examined. Also, in order to build more complex optoelectronic systems and packages, it is now clear that powerful CAD systems capturing both electronic circuits and sub systems as well as optoelectronic and optical components and sub-systems must be made available. Such a CAD system is not only essential for the optoelectronics sub-system designer but also for the electronics system designer. Furthermore, with the scaling of CMOS circuits, in order to conserve drive voltage compatibility, optoelectronic devices that require very low drive voltages are required. Finally, the cost associated with FSOI is of prime concern. The main cost factors include the optoelectronic devices and their integration as well as the overall packaging. The device costs can only be reduced with manufacturing volume. Therefore it is critical to direct the use of optoelectronic arrays to markets with large volumes including optical data storage and bio-photonics. Further in the future, flip-chip bonding with its associated parasitics and high cost should be replaced with heterogeneous integration technologies at the device and material levels rather than at the chip level. Such technologies have the potential to relieve present layout constraints and ultimately reduce cost.

4 Conclusions

Significant progress both at the device and sub-system levels has been made in FSOI to the point where FSOI can now be considered to push the envelope in computing hardware at the board to board interconnect level. However, at the chip to chip level considerable amount of research and development effort still needs to be conducted. Some of the promising new directions that are being investigated at UCSD include the use of 3-D silicon stacks in conjunction with MEMs devices, Conical tapered lens arrays for increased alignment tolerance [17] ,Chatoyant as a versatile CAD system for optoelectronics [18], Ultra low drive surface normal light modulators based on the VCSEL structure [19] and Electric-field assisted micro-assembly and pick and place for advanced integration [20].

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