# Optoelectronic-VLSI Technology: Terabit/s I/O to a VLSI Chip

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The concept of a manufacturable technology that can provide parallel optical interconnects directly to a VLSI circuit, proposed over 15 years ago in [1], now appears to be a reality. One such optoelectronic-VLSI (OE-VLSI) technology is based on the hybrid flip-chip area-bonding of GaAs/AlGaAs Multiple-Quantum Well (MQW) electro-absorption modulator devices directly onto active silicon CMOS circuits. The technology has reached the point where batch-fabricated foundry shuttle incorporating multiple OE-VLSI chip designs are now being run [2]. These foundry shuttles represent the first delivery of custom-designed CMOS VLSI chips with surface-normal optical I/O technology. From a systems point of view, this represents an important step towards the entry of optical interconnects in that: the silicon integrated circuit is state-of-the-art; the circuit is unaffected by the integration process; and the architecture, design, and optimization of the chip can proceed independently of the placement and bonding to the optical I/O.

To date, over 5760 MQW modulator devices have been integrated onto a single CMOS IC with a device yield exceeding 99.95%. Each bonded device has a load capacitance of approximately 50fF (65fF including a 15μmx15μm bond pad) and can be driven by a CMOS inverter to accomplish the electrical-to-optical interface. Compact CMOS transimpedance receiver circuits have been developed to execute the photocurrent-to-logic-level voltage conversion. Operation of single-ended receivers [3] (one diode per optical input) fabricated in a 0.35μm linewidth CMOS technology, has been demonstrated over 1Gigabit/s with a measured bit-error-rate less than $10^{-10}$. Differential two-beam receiver, have similarly been operated to over 1Gbit/s. The

receiver circuits mentioned above have static power dissipation in the range of 3.5-8mW per receiver. More recently, arrays of up to 256 active light sources known as Vertical-Cavity Surface-Emitting Lasers (VCSELs) have also been bonded directly to CMOS VLSI chips [4], with each VCSEL capable of over 1Gigabit/s modulation by the CMOS circuits.

Before such a technology can be deployed on a large scale, several issues related to the scalability of the optoelectronic technology and its compatibility with deep sub-micron CMOS technologies must be addressed. In terms of the modulator technology, the challenges are in reducing the drive voltages of the modulators to stay compatible with sub-micron CMOS technologies, and to continue to improve the yield in the manufacturing and hybridizing of the MQW diodes. In terms of the VCSELs, the challenge will be in producing arrays of power-efficient VCSELs that can attached to CMOS circuits with high-yield, and be simultaneously operated at high speeds [5]. In terms of the circuits, the challenges will be to continue to improve receiver sensitivity while reducing power dissipation and cross-talk. A final consideration is that of the systems integration, where the challenge will be to package systems that can efficiently transport large arrays of light-beams to and from such chips.

Based on relatively conservative assumptions on how these components will evolve, a general conclusion is that it appears this hybrid optical I/O technology has substantial room for continued scaling to large numbers of higher-speed interconnects [6]. Indeed, future OE-VLSI technologies (whether modulator-based or VCSEL-based) can be expected to provide an I/O bandwidth to a chip that is commensurate with the processing power of the chip, even in the finest linewidth silicon: a task that cannot be expected from conventional electrical interconnect technologies. Initial work on space-division crossbar OE-VLSI switches have suggested that terabit capacities are achievable. The availability of optical access to high-speed RAM [7] will also permit the development of shared-memory (SRAM)-based switches: a goal that cannot be achieved with conventional space-division photonic switching technologies. It is anticipated that the availability of such an OE-VLSI technology

will enable terabit-per-second throughput switches with power dissipations on the order of 20-50mW per Gigabit/s of switch throughput.

## References:


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