Pulse-Modulated Vision Chips with Versatile-Interconnected Pixels

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Abstract. This paper proposes and demonstrates novel types of vision chips that utilize pulse trains for image processing. Two types of chips were designed using 1.2 μm double-metal double-poly CMOS process; one is based on a pulse width modulation (PWM) and the other is based on a pulse frequency modulation (PFM). In both chips the interaction between the pixels were introduced to realize the image pre-processing. The basic experimental and simulation results are shown for the PWM and PFM chips, respectively. Also the comparison between two types is discussed.

1 Introduction

A vision chip is a kind of image sensors in which some functional circuits are integrated with a photodetector in each pixel. Several types of vision chips have been reported so far [1]. Because of employing pre-processing in the pixel stage, a vision chip has advantages over a charge-coupled device (CCD) in a viewpoint of fast and versatile image pre-processing.

Viewed in a point of signal processing, they are classified into an analog type and a digital type. The former is more sensitive to noise and has less precision, while the latter has more space-consumed. Pulse modulation is another type [2], where an output signal from a photodiode is converted into a pulse train such as pulse amplitude modulation (PAM), pulse width modulation (PWM), pulse frequency modulation (PFM), pulse phase modulation (PPM), and so on. Except in PAM, all the others are used digital values for output representation as shown in Fig. 1. Thus, in nature the pulse modulation is robust in the signal transmission and well compatible with digital logic circuits. These features are very effective in vision chips where an image pre-processing function is integrated in each pixel.

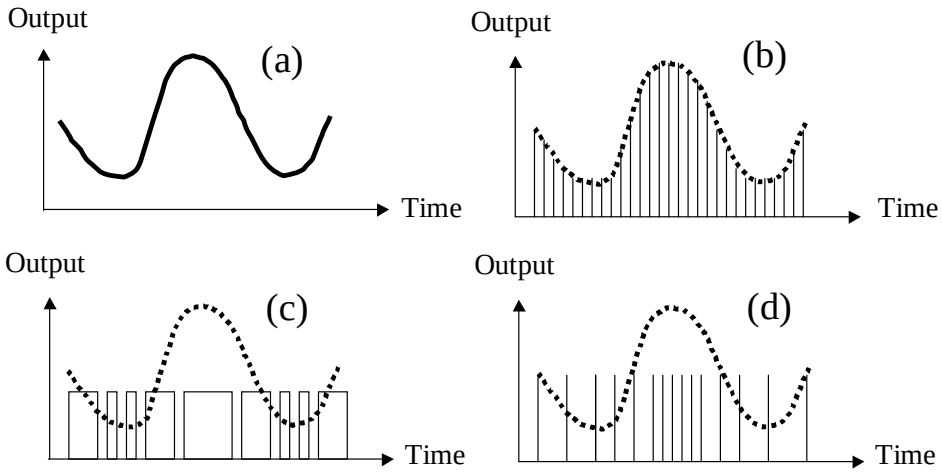

Fig. 1. Schematic of pulse modulation scheme. (a) original analog signal, (b) pulse amplitude modulation, (c) pulse width modulation, (d) pulse frequency modulation.

It is thus crucial issue for vision chips in the next generation to realize the interaction between pixels using pulse modulation scheme. To explore this issue, we propose and demonstrate two types of vision chips employing PWM and PFM. Focusing on implementing inter-pixel connections using pulse trains, we discuss the comparison between two types.

2 Vision Chip Based on PWM

Figure 2 shows circuit diagram of the fabricated PWM vision chip. The circuits consist of a photodiode (PD), a reset transistor M1, a comparator (COMP), and resistive interconnections. The voltage V_{PD} of the floated photodiode PD, which is charged to near V_{dd}, through M1, decreases because the input light discharges the stored charge in the photodiode capacitor C_{PD}. At $t = t_o$ when $V_{PD} < V_{ref}$, the comparator COMP turns on. Here V_{ref} is the reference voltage in COMP. If the output keeps high state or "HI" during the interval, the pulse width T corresponds to the input light intensity. If the change of C_{PD} by the bias voltage is neglected, T is given as follows,

$$T = C_{PD}(V_{reset} - V_{ref}) / I_{ph}. \quad (1)$$

Here I_{ph} is the photocurrent through PD. While in most vision chips as well as conventional image sensors the photodiode voltage V_{PD} is sensed and outputted in a given time, in the PWM the time for reaching a given voltage is sensed and outputted [3], [4].

An inverter with canceling the threshold is used as the comparator COMP as shown in Fig. 3. The reference voltage V_{ref} corresponds to the threshold voltage of the inverter, which is equal to about a half of the supply voltage to the inverter V_{dd}.

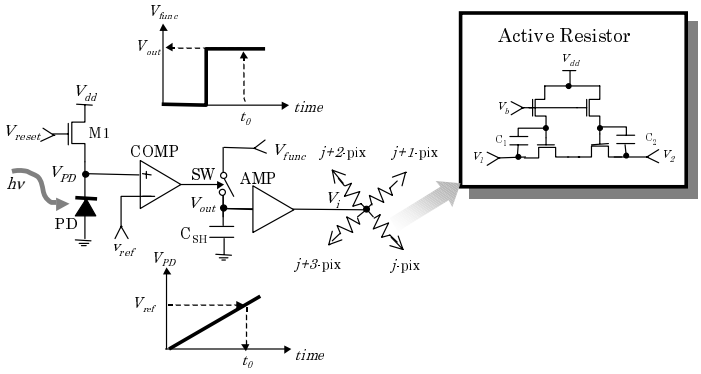

Fig. 2. Circuit diagram of one pixel in a PWM chip.

We employed arbitrary input-output transformation by controlling the switch SW with the output voltage of COMP. The transformation results from the time-dependent voltage of $V_{func}=V_{func}(t)$. When COMP is "HI", SW is ON and C_{SH} is charged through V_{func}. At $t = t_0$ when $V_{PD} < V_{ref}$, the output of COMP is low state or "LO", then SW is OFF and V_{out} is equals to the value of V_{func} at $t = t_0$. In the case of the inset in Fig. 2, we choose the transformation function as binarization by choosing the step function as V_{func}. We can realize any transformation in the relationship between the output voltage and input light intensity by choosing the time-dependence of $V_{func}(t)$.

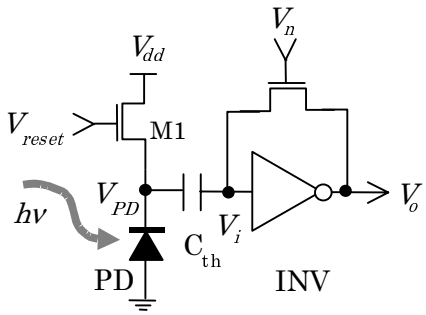

Fig. 3. Circuit diagram of the inverter with canceling the threshold. This is used as the comparator.

As described in the introduction, processing between the nearest neighboring pixels is essential to vision chips. It is difficult to use the output of PWM as it is for

the nearest neighboring processing. Thus each pulse width is converted into an analog value by using the sample-and-hold circuits and then transferred into resistive network through the buffered amp AMP. The capacitance C_{SH} in the sample-and-hold is 220 fF. Resistive network is effective in image processing such as blurring, edge extraction, motion detection, and so on [5]. In our chip, the active resistor is realized as shown in the inset of Fig.4. The capacitors C_1 and C_2 are used to keep the gate voltage constant to the source voltage, which makes the linearity better. This resistor acts in the saturation region and has around 10 kΩ from 0 to 1 V.

The test chip was fabricated with 1.2 μm 2-poly 2-metal CMOS process. The pixel has the area of 158 μm × 163 μm, where 49 transistors are integrated. The photodiode is a parasitic diode with N-well and P-substrate. The fill-factor is 5 %. The number of pixels is 16 × 16. The microphotographs are shown in Fig. 4.

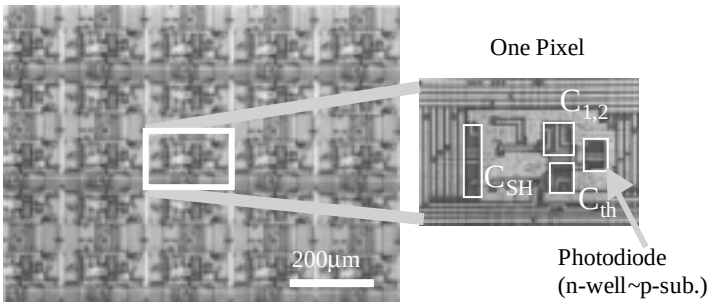

Fig. 4. The microphotographs of the PWM chip and one pixel.

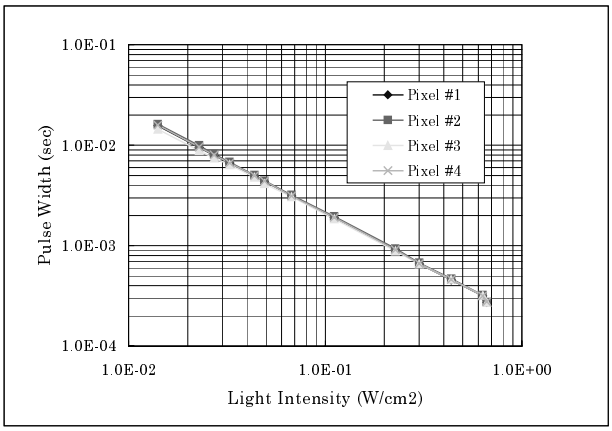

Fig. 5. The pulse width as a function of the input light intensity in different pixels.

The pulse width was measured as a function of the light intensity in the fabricated chip. The pulse width decreases in the inverse proportion to the light intensity, which agrees with Eq. (1). A red LED with the central wavelength of 630 nm was used as

the light source. V_{reset} and V_{ref} are set 3.16V and 1.8 V, respectively. Figure 5 shows the experimental results within 4 pixels, which demonstrates the relative variation of the pulse width was less than 5 %.

Figure 6 shows the similar experimental results as in Fig. 5. In this case the parameter is the power supply voltage to the comparator. As mentioned above, the inverter was used as the comparator, thus the reference voltage was about a half of the supply voltage. This results shows the variation of the pulse width changes only less than 10 % when V_{dd} changes from 2 to 5 V, which shows the effectiveness of this circuit. We are now testing the transformation circuits and the neighboring processing circuits.

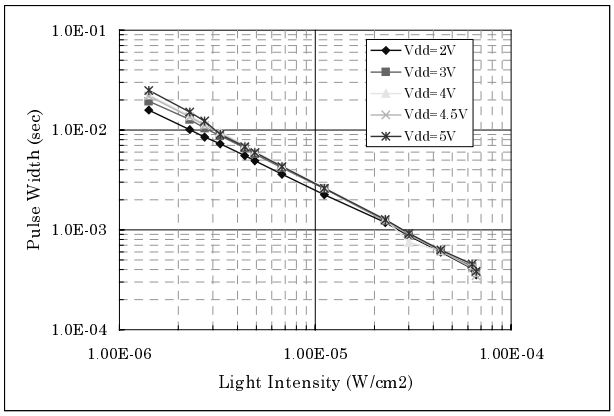

Fig. 6. The pulse width as a function of the input light intensity in different power supply voltages.

3 Vision Chip Based on PFM

A PFM is an output representation that an analog output is converted into pulse frequency, and is used in the output from the nerve cells as spikes. To employ a PFM in a vision chip, relaxation oscillation circuits [6, 7] are constructed as shown in Fig.7. The photodiode PD acts as a variable current source controlled by the input light intensity and is charged through the transistor M1. The gate of M1 is switched by the feedback from the Schmidt trigger ST and the inverter INV. In such a configuration the stronger the light intensity is, the higher the pulse frequency is. The analog value of the light intensity is consequently naturally converted into a pulse train as digital signal.

The circuits in Fig. 7 are designed using the same 1.2 μm CMOS process as in the PWM chip. The layout of one pixel is shown in Fig. 8. The size of one pixel is 50 μm $\times$ 50 μm. The number of the pixel are 32 $\times$ 32. The photodiode consists of N-diffusion and P-substrate, which makes the area reduced compared to the PWM chip. The capacitance of the photodiode is 19 fF without the bias.

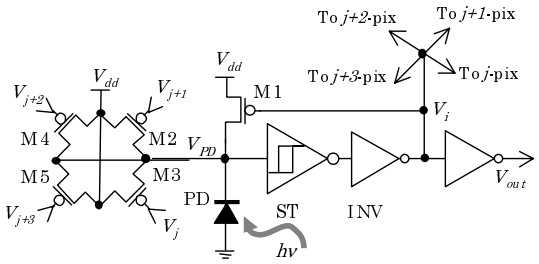

Fig. 7. The circuits diagram of the PFM chip.

Figure 9 shows HSPICE simulation results of output pulse trains from the pixel as shown in Fig. 7. The parasitic capacitances are extracted from the layout shown in Fig. 8. The frequency of the pulse trains is modulated according to the photocurrent, which changes in a ramped manner. The feedback loop to M1 consists of the Schmidt trigger ST that binarizes the output from PD, and the inverter INV for the delay. In this case, the oscillation frequency f is given as

$$f = \frac{I_{ph}}{C_{PD}(V_o - V_{th})}, \tag{2}$$

where V_o is the charge voltage of PD, V_{th} is the threshold voltage of ST. As can be seen from Eq. (2), the frequency f or the firing rate increases if the input light intensity becomes large and the size of PD becomes small.

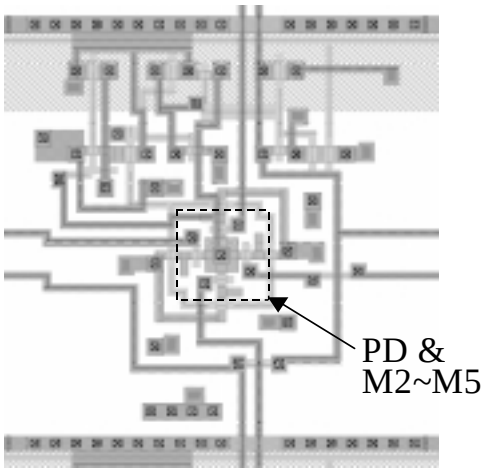

Fig. 8. The layout of one pixel in a PFM chip.

An inhibitory interconnection, which is one of the important functions between neighboring pixels and is much effective in image preprocessing, is realized in a PFM

scheme with very simple circuits as shown in Fig. 7. The additional reset transistors M2 ~ M5 are connected to the PD as well as M1. M2 is switched by the output pulse train from the neighboring pixels and causes the PD charged according to the firing frequency of the neighboring pixels. Thus, the pulse frequency of a pixel is inhibited through the firing frequency of the neighboring pixels. An excitatory connection could be easily realized if the gate signals of M2~M5 are inverted.

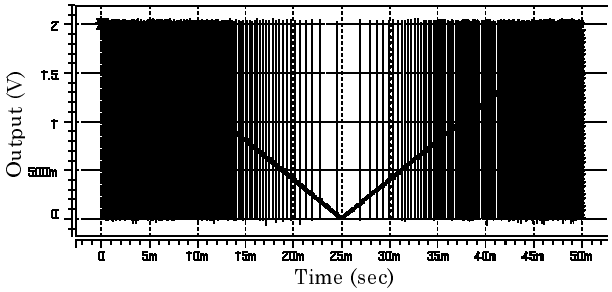

Fig. 9. HSPICE simulation of the pulse stream in a PFM chip. The solid line is the photocurrent, and the dashed line is the output pulses.

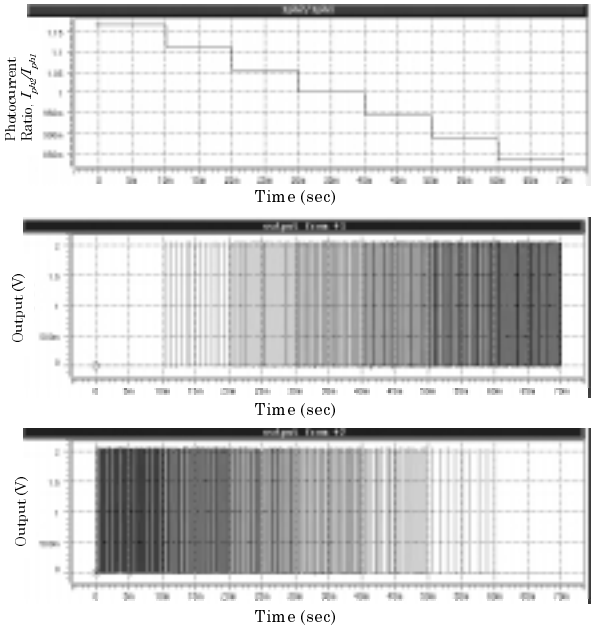

Fig. 10. HSPICE simulation of the mutual inhibitory interconnection in a PFM chip. Upper: photocurrent, middle: output from #1 pixel, bottom: output from #2.

The results of HSPICE simulation for two inhibitory connected pixels are shown in Fig. 10. The power supply voltage is 2 V. In the figure I_{ph1}, the photocurrent in pixel

#1 is kept constant at 1.8 nA while I_{ph2}, one in pixel #2 varying from 2.1 nA to 1.4 nA in a step-like manner. The output pulse trains from pixel #1 and pixel #2 are shown in the middle and the bottom of Fig. 10, respectively. The maximum firing frequency is around 10 kHz. The firing rate in pixel #1 is completely suppressed when I_{ph2}/I_{ph1}=1.2, and gradually increases as I_{ph2}/I_{ph1} decreases. This figure clearly demonstrates that the both firing rates are suppressed each other.

4 Discussion

The PWM represents the information in the rise and fall points of the pulse, which leads to make it easy to use PWM with other logic circuits because of the similar operation manner. Although this is a great advantage over conventional image sensing methods [4], for the neighboring processing such as the resistive network, the conversion to analog values with sample-and-hold is required. This implies the advantage of the pulse scheme is reduced if PWM is employed in vision chips.

As for PFM, we have proposed and demonstrated effective architecture of a vision chip employing PFM. In the architecture, the pulse trains directly affect the state of the neighboring pixels without converting into the analog value. This holds the advantages in the digital manner such as robustness against noise.

Another important feature of the proposed architecture is that decreasing the area of the photodiode little affects the dynamic range. This is confirmed from Eq. (2). It shows that the pulse frequency, which determines the dynamic range, increases if the photodiode capacitance decreases. Consequently it is possible to integrate more functional circuits in each pixel with smaller fill factor. In our chip, the photodiode is designed with the minimum area.

Finally, we discuss the next step of the PFM chip. We have a plan to fabricate the next chip using a deep sub-micron process such as a feature size of 0.25 or 0.18 μm. In such a process, two inevitable issues arise [8]; one is the decrease of the power supply to reduce an electric field applying on a thin oxide layer. The other is that the junction depth for the photodiode becomes shallower. These are detrimental to the dynamic range and the sensitivity for conventional image sensing method. The PFM is one of the candidates for vision chips applicable to a deep sub-micron technology. In that case, parasitic capacitance would be considered more carefully, because it could cause the deviation of the oscillation frequency between pixels.

5 Conclusion

In conclusion, vision chips employing two types of pulse modulation are designed with 1.2 μm CMOS process. In the PWM chip, the interaction between the neighboring pixels is incorporated using the resistive network with the sample-and-hold circuits. The fabricated chip is tested and found to work well in fundamental characteristics. In the PFM chip, mutual inhibitory interconnections are designed and demonstrated in the simulation. The architecture is very simple and suitable to versatile image processing. All digital circuits except for PD makes it possible to use

a conventional logic VLSI fabrication process in the proposed pulsed vision chip. Moreover, the deep sub-micron technology would be applicable to the PFM vision chip.

Acknowledgments

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