

Run-Time Reconfiguration at Xilinx

(invited talk)

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Abstract. Run-Time Reconfiguration (RTR) provides a powerful, but essentially untapped mode of operation for SRAM-based FPGAs. Research over the last decade has indicated that RTR can provide substantial benefits to system designers, both in terms of overall performance and in terms of design simplicity. While RTR holds great promise for many aspects of system design, it has only recently been considered for commercial application. Two factors seem to be converging to make RTR based system design viable. First, silicon process technology has advanced to the point where million gate FPGA devices are commonplace. This permits larger, more complex algorithms to be directly implemented in FPGAs. This alone has led to a quiet revolution in FPGA design. Today, coprocessing using large FPGA devices coupled to standard microprocessors is becoming commonplace, particularly in Digital Signal Processing (DSP) applications. The second factor is software. Until recently, there was literally no software support available for RTR. Existing ASIC-based design flows based on schematic capture and HDL did not provide the necessary mechanisms to allow implementation of RTR systems. Today, the JBits software tool suite from Xilinx provides the direct support for coprocessing and for RTR. The combination of hardware and software for RTR has already begun to show some impressive results on standard system design methodologies and algorithms. Future plans to enhance both FPGA architectures and tools such as JBits should result in a widening acceptance of this technology.