

7th Reconfigurable Architectures Workshop RAW 2000

Workshop Chair

Hossam ElGindy, University of New South Wales (Australia)

Steering Chair

Viktor K. Prasanna, University of Southern California at Los Angeles (USA)

Program Chair

Hartmut Schmeck, University of Karlsruhe (Germany)

Publicity Chair

Oliver Diessel, University of South Australia (Australia)

Programme Committee

Jeff Arnold, Independent Consultant (USA)

Peter Athanas, Virginia Tech (USA)

Gordon Brebner, Univ. of Edinburgh (Scotland)

Andre DeHon, Univ. of California at Berkeley (USA)

Carl Ebeling, Univ. of Washington (USA)

Hossam ElGindy, Univ. of New South Wales (Australia)

Reiner Hartenstein, Univ. of Kaiserslautern (Germany)

Brad Hutchings, Brigham Young Univ. (USA)

Mohammed Khalid, Quickturn Design Systems (USA)

Hyoung Joong Kim, Kangwon National Univ. (Korea)

Rainer Kress, Siemens AG (Germany)

Fabrizio Lombardi, Northeastern University (USA)

Wayne Luk, Imperial College (UK)

Patrick Lysaght, Univ. of Strathclyde (Scotland)

William H. Mangione-Smith, Univ. of California, Los Angeles (USA)

Margaret Marek-Sadowska, Univ. of California, Santa Barbara (USA)

William P. Marnane, Univ. College Cork (Ireland)

Margaret Martonosi, Princeton Univ. (USA)

John T. McHenry, National Security Agency (USA)

Alessandro Mei, Univ. of Trento (Italy)

Martin Middendorf, Univ. of Karlsruhe (Germany)

George Milne, Univ. of South Australia (Australia)

Koji Nakano, Nagoya Institute of Technology (Japan)
Stephan Olariu, Old Dominion Univ. (USA)
Bernard Pottier, Univ. Bretagne Occidentale (France)
Ralph Kohler, Air Force Research Laboratory (USA)
Mark Shand, Compaq Systems Research Center (USA)
Jerry L. Trahan, Louisiana State Univ. (USA)
Ramachandran Vaidyanathan, Louisiana State Univ. (USA)

Preface

The Reconfigurable Architecture Workshop series provides one of the major international forums for researchers to present ideas, results, and on-going research on both theoretical and industrial/ practical advances in Reconfigurable Computing.

The main focus of this year's workshop is "*Run Time Reconfiguration – Foundations, Algorithms, Tools*": Technological advances in the field of fast reconfigurable devices have created new possibilities for the implementation and use of complex systems. Reconfiguration at runtime is one new dimension in computing that blurs the barriers between hardware and software components. Neither the existing processor architectures nor the hardware/software design tools which are available today can fully exploit the possibilities offered by this new computing paradigm. The potential of run time reconfiguration can be achieved through the appropriate combination of knowledge about foundations of dynamic reconfiguration, the various different models of reconfigurable computing, efficient algorithms, and the tools to support the design of run time reconfigurable systems and implementation of efficient algorithms. RAW 2000 provides the chance of creative interaction between these disciplines.

The programme consists of an invited talk by Steven Guccione (Xilinx), technical sessions of refereed papers on various aspects of Run Time Reconfiguration, and a panel discussion on "*The Future of Reconfigurable Computing*". The 12 paper presentations were selected out of 27 submissions after a careful review process, every paper was reviewed by at least three members of the programme committee. We hope that the workshop will provide again the environment for productive interaction and exchange of ideas.

We would like to thank the organizing committee of IPDPS 2000 for the opportunity to organize this workshop, the authors for their contributed manuscripts, and the programme committee for their effort in assessing the 27 submissions to the workshop.

January 2000

Hartmut Schreck

Programme of RAW 2000:

Invited Talk –i title to be inserted!!

Steven A. Guccione

JRoute: A Run-Time Routing API for FPGA Hardware

Eric Keller

A Reconfigurable Content Addressable Memory

Steven A. Guccione, Delon Levi, Daniel Downs

ATLANTIS – A Hybrid FPGA/RISC Based Reconfigurable System

O. Brosch, J. Hesser, C. Hinkelbein, K. Kornmesser, T. Kuberka, A. Kugel, R. Männer, H. Singpiel, B. Vettermann

The Cellular Processor Architecture CEPRA-1X and its Configuration by CDL

Christian Hochberger, Rolf Hofmann, Klaus-Peter Volkmann, Stefan Waldschmidt

Loop Pipelining and Optimization for Run Time Reconfiguration

Kiran Bondalapati, Viktor K. Prasanna

Compiling Process Algebraic Descriptions into Reconfigurable Logic

Oliver Diessel, George Milne

Behavioral Partitioning with Synthesis for MultiFPGA Architectures under Interconnect, Area, and Latency Constraints

Preetham Lakshmikanthan, Sriram Govindarajan, Vinoo Srinivasan, Ranga Vemuri

Module Allocation for Dynamically Reconfigurable Systems

Xuejie Zhang, Kamwing Ng

Augmenting Modern Superscalar Architectures with Configurable Extended Instructions

Xianfeng Zhou, Margaret Martonosi

Complexity Bounds for Lookup Table Implementation of Factored Forms in FPGA Technology Mapping

Wenyi Feng, Fred J. Meyer, Fabrizio Lombardi

Optimization of Motion Estimator for RunTimeReconfiguration Implementation

Camel Tanougast, Yves Berviller, Serge Weber

ConstantTime Hough Transform On A 3D Reconfigurable Mesh Using Fewer
Processors
Yi Pan