The Re-Configurable Delay-Insensitive FLYSIG[1] Architecture[2]

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Abstract: This article describes a new re-configurable architecture design suitable for high performance signal processing applications. The main benefits beside re-configurability are high computation performance, robustness against technology changes, and short design time. Therefore four design paradigms are combined: re-configurable functionality, data-flow orientation, delay-insensitive implementation, and pipelined bit-serial operators. Based on this paradigms a re-configurable high performance processor for cyclic execution of real-time critical algorithms, i.e. a specialized application domain has been designed. Comparable to FPGA based designs operators and interconnections are configurable. In contrast to FPGAs the basic configurable parts are much more complex. This ensures feasibility of complex designs and high complexity The implementation follows a bottom up approach while the concept has been specified top-down.

Overview

Advances in semiconductor technology have opened new dimensions of complexity for integrated circuits. Full custom designs are considered more frequently, if high computation performance is needed. Because time to market shortens more and more it is important to provide hardware prototypes in an early design stage. Re-configurable components as FPGAs have been proven very useful for functional validation. If real-time characteristics and chip area have to be considered, validation based on a re-configurable prototype is only possible if the prototype architecture and the final chip architecture are similar. In general this can not be guaranteed by FPGA components

[1] data**FL**ow oriented dela**Y**-insensitive **SIG**nal processing

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especially if architectures are adapted to specific application domains. We describe an approach providing a re-configurable architecture maintaining the target architecture for the signal processing application domain. Our approach is based on four well known design paradigms brought together for the first time:

- Re-configurable functionality ,
- data-flow oriented architecture design,
- delay-insensitive implementation style, and
- deeply pipelined, bit-serial operator implementation.

Typical applications are real-time control and processing of data-streams, e.g. encoding, decoding, and filters for audio, video, or sensor data. The main benefits of our design approach are re-configurability of operators and interconnection, high performance computation, robustness against technology changes within large limits, and cheap implementation in terms of chip area and design time. The first paradigm, configurable functionality, is well known from FPGA technology. We have added this idea to our approach to support rapid prototyping within short design cycles. The described target architecture is modified by introducing configurable operators and configurable operator interconnection. The result is a prototyping architecture which is in principle identical with the target architecture except for the amount of operators and interconnection possibilities. The concrete target architecture for a successfully prototyped design can be derived easily from the prototyping architecture. The second paradigm, data-flow oriented architecture design [5], adapts the architecture to the class of algorithms in view. The matching of algorithms and architecture is honored by high performance. The third paradigm, delay-insensitive implementation style [1], ensures the robustness against technology changes. We decided to use dual-rail encoding [2] of all signals, so a maximum of robustness can be achieved. Due to the overhead from dual-rail encoding the third paradigm, deeply pipelined bit-serial operator implementation, is involved. The implementation costs of this kind of operators are very low. By pipelining stage parallelism is introduced which leads to high throughput rates. More details are given in [3]. Reasonable improvements in terms of computation performance and reduction of design time are the results from maintaining the structure of the

application for the prototype architecture as well as for the target architecture. The architecture concept is given in Fig.1.

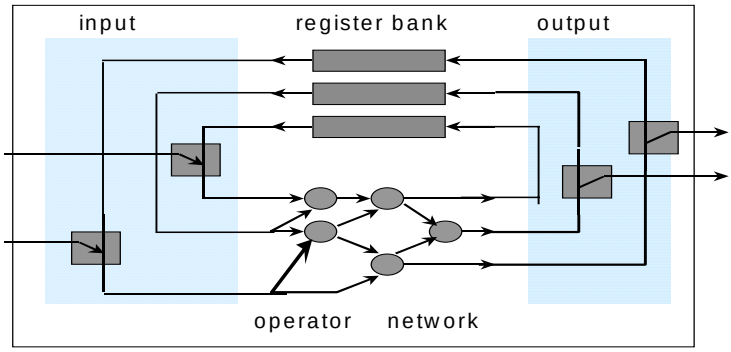

Fig. 1. Data-flow architecture used for implementation of cyclic executed algorithms

To provide re-configurability the two shaded blocks of the FLYSIG architecture (Fig. 1) are implemented by cross bars. This allows the re-configuration of interconnection. In addition the operators of the operator network can be implemented re-configurable. This is especially interesting for operations with similar implementations. We have implemented this architecture for different operator networks. Due to the high flexibility several applications could be mapped onto the same chip. Our approach allows timing analysis and exact estimation of the final chip size during the prototyping design phase. First results show also that the achieved sampling rate (for up to 32 bit data width) is much higher than FPGA technology has provided up to now.

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