

IPPS/SPDP 1999

13th International Parallel Processing Symposium



10th Symposium on Parallel and Distributed Processing

April 12 - 16, 1999

San Juan, Puerto Rico



Keynote Presentations:

K. Mani Chandy, California Institute of Technology
The Changing Nature of Concurrent Computing Research

Burton Smith, Tera Computer Company
The Evolution of Multithreaded Architecture

Barbara Liskov, MIT
Safe Yet Efficient Data Sharing in Wide-Area Distributed Systems

Panel Discussions:

Prospects for High Performance Computing with Java and Middleware
Moderator: Gul Agha, University of Illinois at Urbana-Champaign

Information Power Grid: The New Frontier in Parallel Computing?
Moderator: Vipin Kumar, University of Minnesota

Workshops:

(hew) Heterogeneous Computing Workshop

(hips) Workshop on High-Level Parallel Programming Models and Supportive Environments

(biosp3) Workshop on Biologically Inspired Solutions to Parallel Processing Problems

(wpdrts) Workshop on Parallel and Distributed Real-Time Systems

(rtspp) Workshop on Run-Time Systems for Parallel Programming

(raw) Reconfigurable Architectures Workshop

(java) Workshop on Java for Parallel and Distributed Computing

Workshop on Job Scheduling Strategies for Parallel Processing

(wocs) Workshop on Optics & Computer Science

(ireg) Workshop on Solving Irregularly Structured Problems in Parallel

(pc-now) Workshop on Personal Computer based Networks of Workstations

(fmppa) Workshop on Formal Methods for Parallel Programming: Theory & Applications

(ehpc) Workshop on Embedded HPC Systems and Applications

Workshop on Fault-Tolerant Parallel and Distributed Systems

Workshop on High Performance Data Mining

Tutorials:

Mobile Agents in Distributed Computing (*Monday morning*)

Tutorial on High Performance Data Mining (*Monday afternoon*)

Engineering Web Enabled Systems (*Friday morning*)

Industrial Track/Commercial Exhibits:

FPGA-Based Architecture for High Speed Serial Processing
Paul Kowalewski, Robert L. Donaldson

Delivering on Standards: Balancing Portability and Performance
John Robinson
jrobinson@mc.com

IP Validation for FPGAs using Hardware Object Technology
Steve Casselman, John Schewel, Christophe Beaumont
sc@vcc.com, jas@vcc.com, cb@vcc.com



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ALGORITHMS: Gianfranco Bilardi, Università di Padova and University of Illinois at Chicago
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ARCHITECTURE: Jaswinder Pal Singh, Princeton University
SOFTWARE: Fran Berman, University of California at San Diego

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