



WILDFIRE™ Heterogeneous Adaptive Parallel Processing Systems

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Abstract

The WILDFORCE™ XL card is the newest addition to the WILDFIRE™ family of reconfigurable computing engines. The high-performance WILDFORCE™ XL card takes advantage of the fast, high-capacity, low-power Xilinx XC4000-XL FPGAs (field programmable gate arrays) processing elements. This paper introduces the WILDFORCE™ XL custom computing machine and describes an example application that uses the new technology.

Keywords: FPGA, PCI, CCM, ACS, reconfigurable computing, WILDFIRE, Splash 2, computer architecture, VHDL

1. Introduction

The WILDFORCE™ XL board, shown in Figure 1.1, is the newest member of the WILDFIRE™ family of reconfigurable computing engines. It is in fact a heterogeneous adaptive parallel processing engine simply because it is used to speed up processes normally implemented on a host computer. The methods used to speed up applications include exploiting the inherent parallel-



Figure 1.1 WILDFORCE™ Board

ism in a given algorithm and applying the parallel nature of the WILDFIRE™ boards and Xilinx FPGA (field programmable gate arrays)[7].

The WILDFORCE™ XL performance numbers are shown in Table 1.1.

Table 1.1 WILDFORCE XL Performance Numbers

Max. PE configuration	Five XC4062XL-1s
Usable gates per board	310,000
Max. clock frequency	50 MHz
Max. memory capacity	312 Mbytes
Max. memory bandwidth	1,024 Mbytes/sec
Max. PCI bus bandwidth	120 Mbytes/sec
Max. external I/O bandwidth	900 Mbytes/sec

The WILDFORCE™ XL architecture is described in section 2. The design flow that is followed when writing a WILDFORCE™ XL application is described in section 3. An example application and the speed-up of its implementation on WILDFORCE™ is discussed in section 4. The paper is concluded in section 5.

2. WILDFORCE™ XL architecture

The WILDFORCE™ XL board architecture is based on the WILDFIRE™[4,5] and Splash 2 [1,3] architectures. Advances in host system bus architectures and FPGA technology provide many of the improved performance numbers shown in Table 1.1.

2.1 Inter-PE communications

The WILDFORCE™ XL board is composed of five PEs (processing elements) that are connected by a linear systolic data path and by a crossbar switch, as shown in Figure 2.1. The linear systolic data path is a 36-bit wide bi-directional bus that connects adjacent PEs. The linear systolic path is also used to connect PE1 and PE4 to

their respective FIFO devices or to the external I/O card. The direction of each bit of the linear systolic data path is independently controllable except when used for FIFO communication (where all 36-bits must be configured for input or output).

The crossbar switch provides additional PE interconnectivity. Each PE can be connected to any or all of the other PEs through a single 36-bit crossbar port, except for PE0 which has two such ports. Each crossbar port is divided into nine separate nibble (4-bit) wide slices. The connection and direction of each nibble slice can be controlled.

A set of source and destination port connections for all crossbar port nibbles, when taken together, is called a crossbar configuration. Sixteen of these configurations can be stored in the crossbar at any one time. PE0 is used to select among the sixteen stored crossbar configurations.

In addition to the linear systolic and crossbar data paths, dedicated connections exist between PE0 and each of PEs 1 through 4 (not shown in Figure 2.1). Each of these bi-directional connections is two bits wide.

Every PE is associated with a connector on which can be mounted a mezzanine card fast SRAM or SDRAM. The maximum amount of memory that can supported on the mezzanine card is 64 Mbytes. The PE can read or write 32-bit words from or to the attached memory at a rate of up to 50 MHz.

2.2 Host/PE interface

The WILDFORCE™ XL board is a PCI-based attached-processor card which requires a host computer. Many common PCI-based host systems are supported, including:

- most Intel Pentium-based PCs (running Microsoft Windows NT)
- the DEC Alpha (running Microsoft Windows NT or Digital UNIX)
- Silicon Graphics Origin-200 and Origin-2000 servers (running IRIX v6.x)

The PCI bus allows the WILDFORCE™ XL board to act as both bus initiator and target, thus supporting data transfer rates up to 132 Mbytes per second [6]. The WILDFORCE™ XL board is able to use up to sixteen separate DMA channels to handle host-to-board, board-to-host, and board-to-board data transfers. The on-board DMA channels allow for hand-off data transfers by the host computer.

The host interface to the WILDFORCE™ XL board is composed of separate parts:

- FIFO interface to PE0, PE1, and PE4
- Dual-port memory interface to all PEs
- Local-bus access to all PEs
- Interrupt interface to all PEs

The FIFO interface between the host and PEs 0, 1 and 4 is a 36-bit wide, bi-directional data path. Each FIFO device is composed of two independently operated 512-

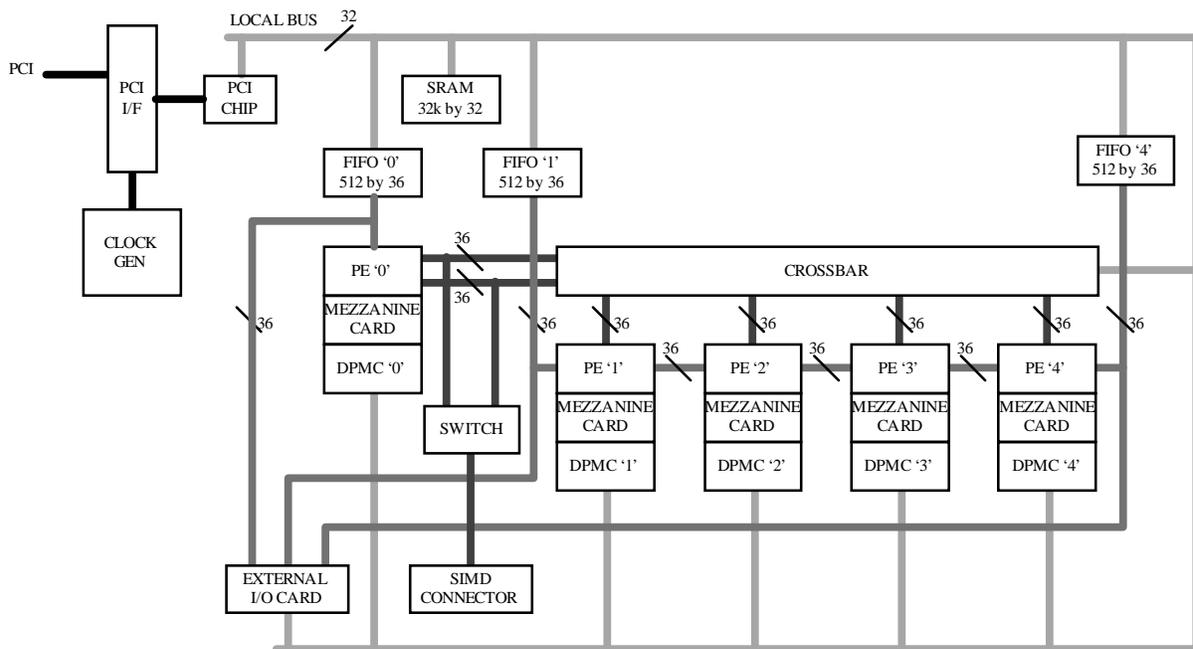


Figure 2.1 WILDFORCE™ XL architectural block diagram.

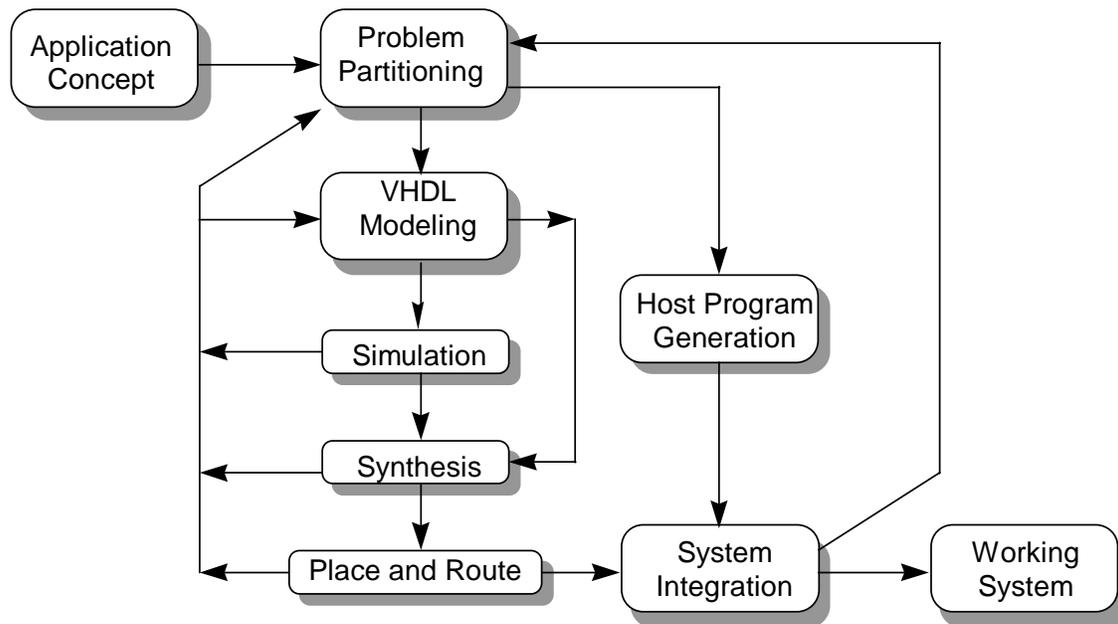


Figure 3.1 WILDFORCE™ XL application design flow diagram

word FIFOs that share one port at either end.

The host can also access each PE's attached memory via the Dual-Port Memory Controller (DPMC). The DPMC effectively turns the single ported memory into a dual-port memory by handling arbitration between host and PE memory access requests.

Registers and memory inside the PE can be accessed directly by the host via the DPMC. This type of direct PE access can be used to load values into the PE without having to reconfigure the PE. It can also be used to read the values of registers or memory internal to the PE for debugging or decision making purposes.

An interrupt mechanism exists in order to provide the PE a means of asynchronously notifying the host of events. The interrupt interface reduces the need for the host side of the application to spend valuable time polling the board.

2.3 External I/O interfaces

In addition to sending data to and from the host, the WILDFORCE™ card is capable of transmitting and receiving data to and from an external source. The interfaces to these external sources include the SIMD connector and the external I/O card connector, both shown in Figure 2.1. The SIMD connector is 36 bits wide and connects to either of PE0's crossbar ports. The external I/O connector has 108 bits split into 3 separate 36-bit ports attached to PE0, PE1, and PE4.

Several types of external I/O cards are available that provide the following interfaces:

- COHU 4110 digital camera input and VGA output

- analog camera input (NTSC, PAL, and SECAM compatible) and VGA output
- 8-channel E1 input/output
- 8-channel T1 input/output
- 2-channel E3 input/output
- 2-channel T3 input/output
- 16-channel RS-422 input/output
- 72-bit linear systolic array input/output

In addition to these off-the-shelf cards, users can build customized I/O cards to fit the published external interface specification of the WILDFORCE™ XL board.

3. Application Design Flow

The standard technique for programming the WILDFIRE™ Reconfigurable Computing Engines involves designing a custom hardware implementation which will perform the desired calculation and then describing the implementation using either a hardware description language or a schematic entry tool. The design flow is shown in Figure 3.1.

Using a hardware description language like Verilog or VHDL allows the design to be simulated in order to test functionality before synthesizing. A behavioral VHDL model of the entire WILDFORCE™ XL system is provided with the board in order to facilitate this verification phase. Once assured of a proper design, the programmer may then synthesize from the high level description to an intermediate format. Xilinx-specific tools then read the intermediate format and produce

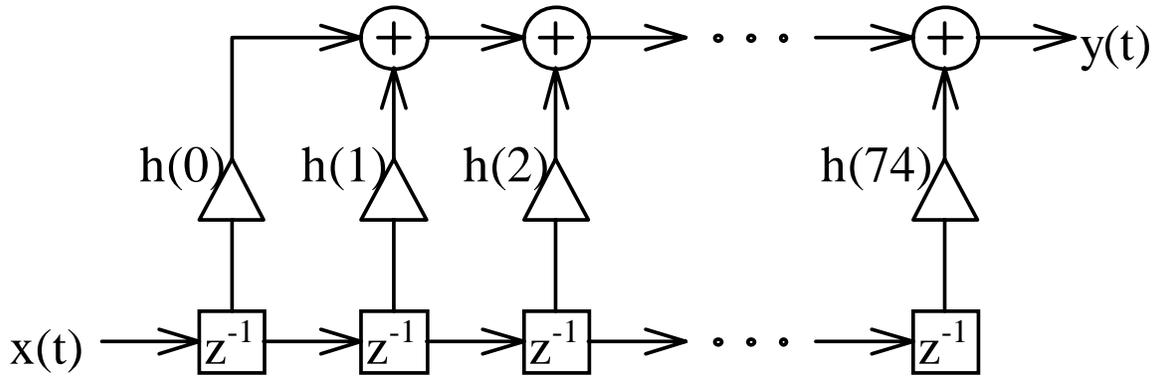


Figure 4.1 Signal-flow graph of a 75-tap FIR filter

binary data suitable for feeding the WILDFIRE™ system.

A host program is then written to configure and control the data flow to and from the WILDFORCE™ XL board. The host part of the program is generated using standard C-programming tools and techniques. A library of WILDFORCE™ API functions is provided to configure and send/receive data to/from the board.

Designing custom hardware for a particular computation involves paying particular attention to details such as the desired number of bits of accuracy, the incoming data rate, and the need to map memory regions into the available memories attached to each PE. Much of the computational advantage of reconfigurable computing engines is derived from the parallelism achieved when a computation is implemented in the form of a deep pipeline.

Highly parallelizable computations whose calculation will fit entirely within the WILDFIRE™ architecture can produce one result per clock cycle. Disadvantages include the need to create custom units for each computation and the potential that a particular design may be too large or too complex to fit on the processing platform. As the area of reconfigurable computing grows, however, these disadvantages are fading quickly with the advent of standard libraries of computational units becoming available to the programmers and the exponentially increasing size of FPGAs.

Also, as the field expands, more tools are becoming available to ease the programming of reconfigurable architectures. Tools which allow programming in high-level languages approaching the general-purpose nature of ANSI-C are being developed. Ultimately, the goal of such tools is to allow reconfigurable architectures to be easily programmed in conjunction with the host processor.

4. Example Application

As an example application, consider a 75-tap FIR filter. The mathematical representation of the output of the filter is as follows:

$$y(t) = \sum_{i \in [0..74]} x(t-i) \cdot h(i)$$

For each input point $x(t)$, 75 multiplications and 74 additions are required to generate the output point $y(t)$. The standard, general-purpose processor, implementation of this calculation involves a loop construct containing two memory accesses, a multiplication, and an addition. Assuming 16-bit data, an unloaded Pentium-II 266 system can perform this operation in about 2.7 microseconds. In contrast, a similar implementation on the WILDFORCE™ XL architecture (in particular, a 4062XL card) can achieve one result every 20 nanoseconds, for a speedup factor of 135.

The signal flow graph for the calculation is shown in Figure 4.1. The highly regular and parallelizable structure can be broken into five equal sections consisting of 15 multipliers and adders, which fit nicely within each processing element of a 4062-XL-based WILDFORCE™ board. Data flow paths of 16 bits for input data and 16 bits for partial results fit comfortably within the 36-bit systolic communication paths. Upon synthesis, the design may be shown to run at a Pclk rate of 50 MHz, producing one result per clock cycle. The parallelism achieved by instantiating 75 separate multiply/accumulate functional units, coupled with the lack of memory accesses necessary due to the ability to register 75 data points, far outweigh the difference in clock speeds from a "meager" 50 MHz on the WILDFORCE™ XL board to the 266MHz operating frequency of the example Pentium-II system.

Similar approaches may achieve high degrees of parallelism in other tasks, such as Fast Fourier Transforms

and other image processing operations[2]. In general, the ability to construct customized functional units from fine-grained computing resources (in this case, Xilinx configurable logic blocks) increases the efficiency of the architecture to such an extent that clock speeds slower than one fifth of a general-purpose microprocessor can still achieve a speedup of more than a hundred.

5. Conclusions and Future Work

The WILDFORCE™ XL reconfigurable computing engine allows the user to easily add custom computing capability to implement highly parallel real-time applications. Annapolis Micro Systems, Inc. is constantly improving the WILDFIRE™ family of reconfigurable computing systems every way. New drivers are being developed to support additional host computers and operating systems. New architectures using the faster, larger, and lower power Xilinx XC4000XV and Virtex FPGAs will provide increased clock rates, higher numbers of gates, and greater PCI and memory bandwidth for more demanding applications.

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