SESSION 1 - Architecture
Chair: Mateo Valero, Universitat Politecnica de Catalunya, Spain

A Study of the Efficiency of Shared Attraction Memories in Cluster-Based COMA Multiprocessors
Anders Landin and Mattias Karlgren, SICS, Sweden
http://www.sics.se/~landin/pub/ippss97/

An Evaluation of a Commercial CC-NUMA Architecture - the CONVEX Exemplar SPP1200
Radhika Thekkath, Amit Pal Singh, Jaswinder Pal Singh, Susan John, and John Hennessy, Stanford University

Coherent Block Data Transfer in the FLASH Multiprocessor
John Heinlein, Kourosh Gharachorloo, Robert P. Bosch, Jr., Mendel Rosenblum, and Anoop Gupta, Stanford University

A Memory Efficient Array Architecture for Real-Time Motion Estimation
Vasily G. Moshnyaga and Keikichi Tamaru, Kyoto University, Japan
http://www.tamaru.kuee.kyoto-u.ac.jp/~vasily/publications.html

An Efficient Technique of Instruction Scheduling on a Superscalar-Based Multiprocessor
Rong-Yuh Hwang, National Taipei Institute of Technology, R.O.C.
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<td>Wide-Sense Nonblocking Clos Networks under Packing Strategy</td>
<td>Yuanyuan Yang and Jianchao Wang</td>
<td>University of Vermont</td>
<td><a href="http://www.emba.uvm.edu/~yang">http://www.emba.uvm.edu/~yang</a></td>
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<td>Gracefully Degradable Pipeline Networks</td>
<td>Robert Cypher and Ambrose K. Laing</td>
<td>Johns Hopkins University</td>
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<td>Distributed Submesh Determination in Faulty Tori and Meshes</td>
<td>Hsing-Lung Chen and Shu-Hua Hu</td>
<td>National Taiwan Institute of Technology, R.O.C.</td>
<td><a href="http://dcs2.et.ntit.edu.tw/">http://dcs2.et.ntit.edu.tw/</a></td>
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<td>Modeling Communication Costs in Multiplexed Optical Switching Networks</td>
<td>C. Salisbury and R. Melhem</td>
<td>University of Pittsburgh</td>
<td><a href="http://www.cs.pitt.edu/~salisbur">http://www.cs.pitt.edu/~salisbur</a></td>
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<td>Characterization of Deadlocks in Interconnection Networks</td>
<td>Sugath Warnakulasuriya and Timothy Mark Pinkston</td>
<td>University of Southern California</td>
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<td>k-ary n-trees: High Performance Networks for Massively Parallel Architectures</td>
<td>Fabrizio Petrini, Universita di Pisa, Italy</td>
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<td><a href="http://www.di.unipi.it/~petrini/petrini.html">http://www.di.unipi.it/~petrini/petrini.html</a></td>
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<td>SuperWeb: Towards a Global Web-Based Parallel Computing Infrastructure</td>
<td>Alberto D. Alexandrov, Maximilian Ibel, Klaus E. Schauser, and Chris J. Scheiman</td>
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<td>S-Check: A Tool for Tuning Parallel Programs</td>
<td>Robert Snelick, National Institute of Standards and Technology</td>
<td><a href="http://www.scheck.nist.gov/scheck/publications.html">http://www.scheck.nist.gov/scheck/publications.html</a></td>
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<td>Interactive Visual Exploration of Distributed Computations</td>
<td>Delbert Hart, Eileen Kraemer, and Gruia-Catalin Roman, Washington University in St. Louis</td>
<td><a href="http://swarm.cs.wustl.edu/cgi-bin/reports.cgi">http://swarm.cs.wustl.edu/cgi-bin/reports.cgi</a></td>
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<td>Fault-Tolerant Deadline-Monotonic Algorithm for Scheduling Hard-Real-Time Tasks</td>
<td>Alan A. Bertossi, Andrea Fusiello, and Luigi Mancini, Universita di Trento, Italy</td>
<td><a href="http://rtm.science.unitn.it/~fusiello/ipps97-121/ipps97.ps">http://rtm.science.unitn.it/~fusiello/ipps97-121/ipps97.ps</a></td>
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<td>Performance Comparison of Processor Scheduling Strategies in a Distributed-Memory Multicomputer System</td>
<td>Yuet-Ning Chan, Sivarama P. Danadmudi, and Shikharesh Majumdar, Carleton University, Canada</td>
<td><a href="http://www.scs.carleton.ca/scs/tech_reports/1997/list.html">http://www.scs.carleton.ca/scs/tech_reports/1997/list.html</a></td>
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<td>Optimal Scheduling for UET-UCT Generalized n-Dimensional Grid Task Graphs</td>
<td>Theodore Andronikos, Nectarios Koziris, George Papakonstantinou, and Panayotis Tsanakas, National Technical University of Athens, Greece</td>
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<td>A Comparison of General Approaches to Multiprocessor Scheduling</td>
<td>Jing-Chiou Liou and Michael A. Palis, AT&amp;T Laboratories, Middletown</td>
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<td>DFRN: A New Approach on Duplication Based Scheduling for Distributed Memory Multiprocessor Systems</td>
<td>Gyung-Leen Park, Behrooz Shirazi, and Jeff Marquis, The University of Texas at Arlington</td>
<td><a href="http://zeus.uta.edu/~web_site">http://zeus.uta.edu/~web_site</a></td>
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<td>Dynamic Processor Scheduling with Client Resources for Fast Multi-resolution WWW</td>
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**SESSION 5 - Applications**

Chair: Josep Diaz, Universitat Politencnica de Catalunya, Spain

**Performance Analysis and Optimization on a Parallel Atmospheric General Circulation Model Code**
John Z. Lou and John D. Farrara, Jet Propulsion Laboratory
http://olympic.jpl.nasa.gov/PERSONNEL/lou/

**A Tool for On-Line Visualization and Interactive Steering of Parallel HPC Applications**
Sabine Rathmayer and Michael Lenke, Technische Universitat Munchen, Germany
http://wwwbode.informatik.tu-muenchen.de/~maiers/

**Performance Prediction for Complex Parallel Applications**
Jürgen Brehm and Patrick Worley, Institut fur Rechnerstrukturen und Betriebssysteme, Germany
http://www.irb.uni-hannover.de/~brehm/publications/publications.html

**Implementation and Results of Hypothesis Testing from the C³I Parallel Benchmark Suite**
Brian VanVoorst, Luiz Pires, Rakesh Jha, and Mustafa Muhhamad, Honeywell Technology Center
http://www.se.rl.af.mil:8001

**Real-Time Parallel MPEG-2 Decoding in Software**
Angelos Bilas, Jason Fritts, and Jaswinder Pal Singh, Princeton University
http://www.cs.princeton.edu:80/~bilas/

**Parallel Inference on a Linguistic Knowledge Base**
Sanda M. Harabagiu and Dan I. Moldovan, University of Southern California
http://www-scf.usc.edu/~harabagi/

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**SESSION 6 - Performance Evaluation**

Chair: Jose D.P. Rolim, University of Geneva

**Predicting Queue Times on Space-sharing Parallel Computers**
Allen B. Downey, University of California, Berkeley
DPF: A Data Parallel Fortran Benchmark Suite
Yu Hu, Lennart Johnsson, Dimitris Kehagias, and Nadia Shalaby, Harvard University
http://www.das.harvard.edu/cs/research/dpf/root.html

Latency Tolerance: A Metric for Performance Analysis of Multithreaded Architectures
Shashank S. Nemawarkar and Guang R. Gao, McGill University, Canada
http://www-acaps.cs.mcgill.ca/~shashank

Architecture and Performance of the Hitachi SR2201 Massively Parallel Processor System
Hiroaki Fujii, Yoshiko Yasuda, Hideya Akashi, Yasuhiro Inagami, Makoto Koga, Osamu Ishihara, Masamori Kashiyama, Hideo Wada, and Tsutomu Sumimoto, Hitachi, Ltd., Japan

Experience with Fine-Grained Communication in EM-X Multiprocessor for Parallel Sparse Matrix Computation
Mitsuhisa Sato, Yuetsu Kodama, Hirofumi Sakane, Hayato Yamana, Shuichi Sakai, and Yoshinori Yamaguchi, Tsukuba Research Center, Japan
http://www.rwcp.or.jp/lab/mpperf/papers/ipps97.ps.gz

A Customizable Simulator for Workstation Networks
Mustafa Uysal, Anurag Acharya, Robert Bennett, and Joel Saltz, University of Maryland

SESSION 7 - Synchronization and Threads
Chair: Kai Li, Princeton University

Empirical Evaluation of Distributed Mutual Exclusion Algorithms
Shiwa S. Fu, Nian-Feng Tzeng, and Zhiyuan Li, University of Southwestern Louisiana
http://www.usl.edu/~ssf/ipps97.ps

External Adjustment of Runtime Parameters in Time Warp Synchronized Parallel Simulators
Radharamanan Radhakrishnan, Lantz Moore, and Philip A. Wilsey, University of Cincinnati
http://www.ececs.uc.edu/~paw/

Relative Performance of Preemption-Safe Locking and Non-Blocking Synchronization on Multiprogrammed Shared Memory Multiprocessors
Maged M. Michael and Michael L. Scott, University of Rochester
http://www.cs.rochester.edu/u/michael

A Reliable Hardware Barrier Synchronization Scheme
Rajeev Sivaram, Craig B. Stunkel, and Dhabaleswar K. Panda, IBM T.J. Watson Research Center
Analysis of Several Scheduling Algorithms under the Nano-Threads Programming Model
Xavier Martorell, Jesus Labarta, Nacho Navarro, and Eduard Ayguade, Universitat Politecnica de Catalunya (UPC), Spain
http://www.ac.upc.es/~xavim/Home.html

Comparing Gang Scheduling with Dynamic Space Sharing on Symmetric Multiprocessors Using Automatic Self-Allocating Threads (ASAT)
Charles Severance and Richard Enbody, Michigan State University

SESSION 8 - Algorithms I
Chair: Sanguthevar Rajasekaran, University of Florida

A Randomized Sorting Algorithm on the BSP model
Alexandros V. Gerbessiotis and Constantinos J. Siniolakis, Oxford University, United Kingdom
http://www.comlab.ox.ac.uk/oucl/users/alex.gerbessiotis/ipps97.ps.gz

Work-Time Optimal k-merge Algorithms on the PRAM
Tatsuya Hayashi, Koji Nakano, and Stephan Olariu, Nagoya Institute of Technology, Japan
http://maple.elcom.nitech.ac.jp/~nakano

Optimizing Parallel Bitonic Sort
Mihai F. Ionescu and Klaus E. Schauser, University of California, Santa Barbara

A Fast Scalable Universal Matrix Multiplication Algorithm on Distributed-Memory Concurrent Computers
Jaeyoung Choi, Soongsil University, Korea
http://comp.soongsil.ac.kr/~jchoi.html

Matrix Transpose on Meshes: Theory and Practice
Michael Kaufmann, Ulrich Meyer, and Jop Sibeyn, Max-Planck-Institut fur Informatik, Germany
http://www.mpi-sb.mpg.de/~jopsi

Coarse Grained Parallel Next Element Search
Albert Chan, Frank Dehne, and Andrew Rau-Chaplin, Carlton University, Canada
http://www.scs.carleton.ca/~dehne/
SESSION 9 - Routing
Chair: Gianfranco Bilardi, Universita di Padova and University of Illinois at Chicago

**Optimal Wormhole Routing in the (n,d)-Torus**
Stefan Bock, Friedhelm Meyer auf der Heide, and Christian Scheideler, University of Paderborn, Germany
http://www.uni-paderborn.de/cs/fmadh.html

**Adaptive Fault-Tolerant Wormhole Routing Algorithms for Hypercube and Mesh Interconnection Networks**
Jau-Der Shih, National Pintung Teachers College, R.O.C.

**A Hybrid Interconnection Network for Integrated Communication Services**
Yi-long Chen and Jyh-Charn Liu, Texas A&M University

**Deadlock-free Fault-tolerant Routing in the Multi-dimensional Crossbar Network and its Implementation for the Hitachi SR2201**
Yoshiko Yasuda, Hiroaki Fujii, Hideya Akashi, Yasuhiro Inagami, Teruo Tanaka, Junji Nakagoshi, Hideo Wada, and Tsutomu Sumimoto, Hitachi, Ltd., Japan

**An Accurate Model for the Performance Analysis of Deterministic Wormhole Routing**
B. Ciciani, M. Colajanni, and C. Paolucci, Universita di Roma "La Sapienza", Italy

SESSION 10 - I/O and Message Passing
Chair: Anthony Skjellum, Mississippi State University

**Design and Evaluation of a Data Storage and Retrieval Strategies in a Distributed Memory Continuous Media Server**
Chutimet Srinilta, Divyesh Jadav, and Alok Choudhary, Syracuse University
http://www.ece.nwu.edu/~csrinilt

**MTIO A Multi-Threaded Parallel I/O System**
Sachin More, Alok Choudhary, Ian Foster, and Ming Q. Xu, Northwestern University
http://www.ece.nwu.edu/~ssmore/ipps97.ps

**Low Latency MPI for Meiko CS/2 and ATM Clusters**
Chris R. Jones, Ambuj K. Singh, and Divyakant Agrawal, University of California, Santa Barbara
http://www.cs.ucsb.edu/~agrawal

**Reducing Waiting Costs in User-Level Communication**
Stefans N. Damianakis, Yuqun Chen, and Edward W. Felten, Princeton University
Design and Implementation of Virtual Memory-Mapped Communication on Myrinet
Cezary Dubnicki, Angelos Bilas, Kai Li, and Jim F. Philbin, NEC Research Institute

SESSION 11 - Algorithms II
Chair: Tao Yang, University of California at Santa Barbara

Designing Efficient Distributed Algorithms Using Sampling Techniques
Sanguthevar Rajasekaran and David S.L. Wei, University of Florida

Fast Parallel Computation of the Polynomial Shift
Eugene V. Zima, Moscow State University, Russia
http://www.cs.msu.su/~zima

A Parallel Algorithm for Weighted Distance Transforms
Akihiro Fujiwara, Michiko Inoue, Toshimitsu Masuzawa, and Hideo Fujiwara, Nara Institute of Science and Technology (NAIST), Japan
http://rocana.aist-nara.ac.jp/~tora/

Parallel Solutions of Indexed Recurrence Equations
Yosi Ben-Asher and Gady Haber, Haifa University, Israel

Joining Forces in Solving Large-Scale Quadratic Assignment Problems in Parallel
Adrian Brüngger, Ambros Marzetta, Jens Clausen, and Michael Perregaard, Swiss Federal Institute of Technology, Switzerland
http://wwwjn.inf.ethz.ch/ambros/ipps97_qap_zram.ps.gz

SESSION 12 - Runtime
Chair: Hans Zima, University of Vienna

Optimization Schemas for Parallel Implementation of Nondeterministic Languages and Systems
Gopal Gupta and Enrico Pontelli, New Mexico State University
http://www.cs.nmsu.edu/lldap/prj_lp/opt.html

Logic Channels: A Coordination Approach to Distributed Programming
M. Díaz, B. Rubio, and J.M. Troya, Universidad de Malaga, Spain
http://www.lcc.uma.es/personal/diaz/diaz.html
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<tr>
<td>Time-Stamping Algorithms for Parallelization of Loops at Run-Time</td>
<td>Chengzhong Xu and Vipin Chaudhary, Wayne State University</td>
<td><a href="http://www.pdcl.eng.wayne.edu">http://www.pdcl.eng.wayne.edu</a></td>
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<td>Platform-Independent Runtime Optimizations Using OpenThreads</td>
<td>Matthew Haines and Koen Langendoen, University of Wyoming</td>
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<td>Aurora: Scoped Behavior for Per-Context Optimized Distributed Data Sharing</td>
<td>Paul Lu, University of Toronto, Canada</td>
<td><a href="http://www.cs.utoronto.ca/~paullu">http://www.cs.utoronto.ca/~paullu</a></td>
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Chair: Uzi Vishkin, University of Maryland and Tel Aviv University

**O(\log \log N) Time Algorithms for Hamiltonian-Suffix and Min-Max-Pair Heap Operations on Hypercube Multicomputers**  
Sajal K. Das and M. Cristina Pinotti, University of North Texas

**A Parallel Tabu Search Algorithm for the 0-1 Multidimensional Knapsack Problem**  
Smail Niar and Arnaud Freville, Universite de Valenciennes, France  
[http://www.univ-valenciennes.fr/limav](http://www.univ-valenciennes.fr/limav)

**Lower Bounds on Systolic Gossip**  
Michele Flammini and Stéphane Pérennès, University of L'Aquila, Italy

**Parallel Simulated Annealing: An Adaptive Approach**  
Jonas Knopman and Júlio S. Aude, Federal University of Rio de Janeiro - NCE, Brazil

**Parallel Global Routing Algorithms for Standard Cells**  
Zhaoyun Xing, John Chandy, and Prithviraj Banerjee, University of Illinois at Urbana-Champaign  
[http://www.ece.nwu.edu/~banerjee/](http://www.ece.nwu.edu/~banerjee/)

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### SESSION 15 - Compilers I
Chair: Emilio Zapata, University of Malaga, Spain

**On Privatization of Variables for Data-Parallel Execution**  
Manish Gupta, IBM T.J. Watson Research Center  
[http://www.research.ibm.com/people/g/gupta](http://www.research.ibm.com/people/g/gupta)

**Semantics and Implementation of a Generalized forall Statement for Parallel Languages**  
[http://www.cp.tn.tudelft.nl/paul/](http://www.cp.tn.tudelft.nl/paul/)

**A BSP Approach to the Scheduling of Tightly-Nested Loops**  
Radu Calinescu, Oxford University Computing Laboratory, England  
[http://www.comlab.ox.ac.uk/oucl/users/radu.calinescu/ipps97-paper.ps.gz](http://www.comlab.ox.ac.uk/oucl/users/radu.calinescu/ipps97-paper.ps.gz)

**A Formal Model of Software Pipelining Loops with Conditions**  
Dragan Milicev and Zoran Jovanovic, University of Belgrade, Yugoslavia  
[http://ubbg.etf.bg.ac.yu/~emiliced](http://ubbg.etf.bg.ac.yu/~emiliced)

**Data Access Reorganizations in Compiling Out-of-Core Data Parallel Programs on Distributed Memory Machines**
## SESSION 16 - Networks II
Chair: Timothy Pinkston, University of Southern California

**Hybrid Time Synchronization Implemented Through Special Ring Array for Mesh or Torus**
Yuzhong Sun, Zhiwei Xu, and Mingfa Zhu, National Research Center for Intelligent Computers, P.R.C.

**Deadlock- and Livelock-Free Routing Protocols for Wave Switching**
José Duato, Pedro López, and Sudhakar Yalamanchili, Georgia Institute of Technology

**Architecture-Dependent Tuning of the Parameterized Communication Model for Optimal Multicasting**
Natawut Nupairoj, Lionel M. Ni, Ju-Young L. Park, and Hyeong-Ah Choi, Michigan State University
[http://www.cps.msu.edu/~ni](http://www.cps.msu.edu/~ni)

**Crossbar Analysis for Optimal Deadlock Recovery Router Architecture**
Yungho Choi and Timothy Mark Pinkston, University of Southern California
[http://www.usc.edu/dept/ceng/pinkston/SMART.html](http://www.usc.edu/dept/ceng/pinkston/SMART.html)

**Performance Analysis of Minimal Adaptive Wormhole Routing with Time-Dependent Deadlock Recovery**
Fabrizio Petrini and Marco Vanneschi, Universita di Pisa, Italy
[http://www.di.unipi.it/~petrini/petrini.html](http://www.di.unipi.it/~petrini/petrini.html)

## SESSION 17 - Algorithms IV
Chair: Sajal Das, University of North Texas

**A 2-D Parallel Convex Hull Algorithm with Optimal Communication Phases**
Jieliang Zhou, Xiaotie Deng, and Patrick Dymond, York University, Canada

Chin-Wen Ho, Sun-Yuan Hsieh, and Gen-Huey Chen, Institute of Information Science, R.O.C.
An Efficient Parallel Algorithm for Solving the Knapsack Problem on the Hypercube
A. Goldman and D. Trystram, LMC-IMAG, France

d-Dimensional Range Search on Multicomputers
Afonso Ferreira, Claire Kenyon, Andrew Rau-Chaplin, and Stephane Ubéda, LIP ENS-Lyon, France

Control Schemes in a Generalized Utility for Parallel Branch-and-Bound Algorithms
Yuji Shinano, Kenichi Harada, and Ryuichi Hirabayashi, Science University of Tokyo, Japan
http://hiraws1.ms.kagu.sut.ac.jp/~shinano/index.html

SESSION 18 - Compilers II
Chair: Prith Banerjee, Northwestern University

Alias Analysis for Fortran90 Array Slices
K. Gopinath and R. Seshadri, Indian Institute of Science, India
http://drona.csa.iisc.ernet.in/~gopi/conf/aliasipps97.ps

A Compile-Time Partitioning Strategy for Non-Rectangular Loop Nests
Rizos Sakellariou, University of Manchester, United Kingdom
http://www.cs.man.ac.uk/cnc/staff/rizos/ipps97.ps

The Sparse Cyclic Distribution against its Dense Counterparts
Gerardo Bandera, Manuel Ujaldon, Maria A. Trenas, and Emilio L. Zapata, University of Malaga, Spain

A Compiler-Directed Cache Coherence Scheme Using Data Prefetching
Hock-Beng Lim and Pen-Chung Yew, University of Illinois at Urbana-Champaign

Extensible Message Passing Application Development and Debugging with Python
David M. Beazley and Peter S. Lomdahl, University of Utah
http://www.cs.utah.edu/~beazley/publications.html

SESSION 19 - Architecture Theory
Chair: Ali Hurson, Pennsylvania State University

Parallel 'Go with the Winners' Algorithms in the LogP Model
Marcus Peinado and Thomas Lengauer, German National Research Center for Information
A Comparison of Parallel Approaches for Algebraic Factorization in Logic Synthesis
Sumit Roy and Prithviraj Banerjee, Northwestern University
http://www.ece.nwu.edu/~banerjee/

Conflict-Free Access to Multiple Single-Ported Register Files
Silvia M. Mueller and Uzi Vishkin, University of Saarland, Germany
http://www-wjp.cs.uni-sb.de/~smueller/spv.html

On the Dynamic Initialization of Parallel Computers
Stephan Olariu, Ivan Stojmenovic, and Albert Y. Zomaya, Waterloo University, Canada

SESSION 20 - Data Structures
Chair: Afonso Ferreira, CNRS, LIP - ENS Lyon, France

The Impact of Timing on Linearizability in Counting Networks
Marios Mavronicolas, Marina Papatriantafilou, and Philippas Tsigas, Max-Planck-Institut fur Informatik, Germany

A Parallel Priority Data Structure with Applications
Gerth Stølting Brodal, Jesper Larsson Träff, and Christos D. Zaroliagis, University of Aarhus, Denmark
http://www.mpi-sb.mpg.de/~zaro

Multiple Templates Access of Trees in Parallel Memory Systems
Vincenzo Auletta, Amelia De Vivo, and Vittorio Scarano, Universita di Salerno, Italy
http://www.unisa.it/auletta.dir/PUB/PAPERS/templates.ps

Maintaining Spatial Data Sets in Distributed-Memory Machines
Susanne E. Hambrusch and Ashfaq A. Khokhar, Purdue University
http://www.cs.purdue.edu/people/she

Geometric Data Structures on a Reconfigurable Mesh, with Applications
Amitava Datta, University of New England, Australia
http://turing.une.edu.au/~datta
### SESSION 21 - Networks III

**Chair:** Helmar Burkhart, University of Basel, Switzerland

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<td>Efficient Sorting and Routing on Reconfigurable Meshes Using Restricted Bus Length</td>
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<td>Oblivious Routing Algorithms on the Mesh of Buses</td>
<td>Kazuo Iwama and Eiji Miyano, Kyushu University, Japan</td>
<td><a href="http://hakozaki.csce.kyushu-u.ac.jp/~iwama">http://hakozaki.csce.kyushu-u.ac.jp/~iwama</a></td>
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<td>Nearly Optimal One-to-Many Parallel Routing in Star Networks</td>
<td>Jianer Chen and Chi-Chang Chen, Texas A&amp;M University</td>
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<td>Johanne Cohen, Pierre Fraigniaud, Jean-Claude Konig, and André Raspaud, Ecole Normale Superieure de Lyon, France</td>
<td><a href="http://www.ens-lyon.fr/LIP/groupes/crac/list_member.us.html">http://www.ens-lyon.fr/LIP/groupes/crac/list_member.us.html</a></td>
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<td>Cyclic Networks: A Family of Versatile Fixed-Degree Interconnection Architectures</td>
<td>Chi-Hsiang Yeh and Behrooz Parhami, University of California, Santa Barbara</td>
<td><a href="http://www.engineering.ucsb.edu/~yeh">http://www.engineering.ucsb.edu/~yeh</a></td>
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### Industrial Track - Invited Vendor Presentations

**Co-Chairs:** John K. Antonio, Helmar Burkhart

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<td>SPAX: A New Parallel Processing System for Commercial Application</td>
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