

Author Index

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The authors are listed in alphabetical order by last names. The second column lists the track and topic of the author's paper and are useful in finding other related papers using the [session index](#). The session and paper numbers are useful in finding the postscript version of the paper. For example, "Session 6, #337" means the postscript file named "337.ps" can be found in the subdirectory "ipps97/s6/".

A B C D E F G H I J K L M N O P R S T U V W X Y Z

A

Anurag Acharya	<i>A Customizable Simulator for Workstation Networks</i> Software Track, Performance Evaluation, Session 6, #337
Divyakant Agrawal	<i>Low Latency MPI for Meiko CS/2 and ATM Clusters</i> Architecture Track, I/O and Message Passing, Session 10, #206
Hideya Akashi	<i>Deadlock-free Fault-tolerant Routing in the Multi-dimensional Crossbar Network and its Implementation for the Hitachi SR2201</i> Software Track, Routing, Session 9, #204
Hideya Akashi	<i>Architecture and Performance of the Hitachi SR2201 Massively Parallel Processor System</i> Software Track, Performance Evaluation, Session 6, #383
Alberto D. Alexandrov	<i>SuperWeb: Towards a Global Web-Based Parallel Computing Infrastructure</i> Software Track, Tools, Session 3, #267
Daniel Andresen	<i>Dynamic Processor Scheduling with Client Resources for Fast Multi-resolution WWW Image Browsing</i> Architecture Track, Scheduling, Session 4, #327
Theodore Andronikos	<i>Optimal Scheduling for UET-UCT Generalized n-Dimensional Grid Task Graphs</i> Architecture Track, Scheduling, Session 4, #162
Julio S. Aude	<i>Parallel Simulated Annealing: An Adaptive Approach</i> Algorithm and Application Track, Algorithms III, Session 14, #257
Vincenzo Auletta	<i>Multiple Templates Access of Trees in Parallel Memory Systems</i> Algorithm and Application Track, Data Structures, Session 20, #245

D.R. Avresky	<i>Maximum Delivery Time and Hot Spots in ServerNet™ Topologies</i> Industrial Track, Invited Vendor Presentations, Session IT, #ind3
Eduard Ayguade	<i>Analysis of Several Scheduling Algorithms under the Nano-Threads Programming Model</i> Architecture Track, Synchronization and Threads, Session 7, #217
B	
Gerardo Bandera	<i>The Sparse Cyclic Distribution against its Dense Counterparts</i> Software Track, Compilers II, Session 18, #302
Prithviraj Banerjee	<i>A Comparison of Parallel Approaches for Algebraic Factorization in Logic Synthesis</i> Architecture Track, Architecture Theory, Session 19, #394
Prithviraj Banerjee	<i>Parallel Global Routing Algorithms for Standard Cells</i> Algorithm and Application Track, Algorithms III, Session 14, #284
David M. Beazley	<i>Extensible Message Passing Application Development and Debugging with Python</i> Software Track, Compilers II, Session 18, #251
Yosi Ben-Asher	<i>Parallel Solutions of Indexed Recurrence Equations</i> Algorithm and Application Track, Algorithms II, Session 11, #175
Robert Bennett	<i>A Customizable Simulator for Workstation Networks</i> Software Track, Performance Evaluation, Session 6, #337
Alan A. Bertossi	<i>Fault-Tolerant Deadline-Monotonic Algorithm for Scheduling Hard-Real-Time Tasks</i> Architecture Track, Scheduling, Session 4, #121
Angelos Bilas	<i>Design and Implementation of Virtual Memory-Mapped Communication on Myrinet</i> Architecture Track, I/O and Message Passing, Session 10, #330
Angelos Bilas	<i>Real-Time Parallel MPEG-2 Decoding in Software</i> Algorithm and Application Track, Applications, Session 5, #219
Stefan Bock	<i>Optimal Wormhole Routing in the (n,d)-Torus</i> Software Track, Routing, Session 9, #161
R. Bordawekar	<i>Data Access Reorganizations in Compiling Out-of-Core Data Parallel Programs on Distributed Memory Machines</i> Software Track, Compilers I, Session 15, #233
Robert P. Bosch, Jr.	<i>Coherent Block Data Transfer in the FLASH Multiprocessor</i> Architecture Track, Architecture, Session 1, #313
P. Bose	<i>Accuracy and Speed-Up of Parallel Trace-Driven Architectural Simulation</i> Architecture Track, Architecture, Session 1, #308
L.C. Breebaart	<i>Semantics and Implementation of a Generalized forall Statement for Parallel Languages</i>

Jurgen Brehm *Performance Prediction for Complex Parallel Applications*
Algorithm and Application Track, Applications, Session 5, #178

Gerth Stolting Brodal *A Parallel Priority Data Structure with Applications*
Algorithm and Application Track, Data Structures, Session 20, #174

Adrian Brünger *Joining Forces in Solving Large-Scale Quadratic Assignment Problems in Parallel*
Algorithm and Application Track, Algorithms II, Session 11, #179

C

Radu Calinescu *A BSP Approach to the Scheduling of Tightly-Nested Loops*
Software Track, Compilers I, Session 15, #140

Albert Chan *Coarse Grained Parallel Next Element Search*
Algorithm and Application Track, Algorithms I, Session 8, #128

Yuet-Ning Chan *Performance Comparison of Processor Scheduling Strategies in a Distributed-Memory Multicomputer System*
Architecture Track, Scheduling, Session 4, #129

John Chandy *Parallel Global Routing Algorithms for Standard Cells*
Algorithm and Application Track, Algorithms III, Session 14, #284

Vipin Chaudhary *Time-Stamping Algorithms for Parallelization of Loops at Run-Time*
Software Track, Runtime, Session 12, #223

Yi-long Chen *A Hybrid Interconnection Network for Integrated Communication Services*
Software Track, Routing, Session 9, #278

Yuqun Chen *Reducing Waiting Costs in User-Level Communication*
Architecture Track, I/O and Message Passing, Session 10, #293

Hsing-Lung Chen *Distributed Submesh Determination in Faulty Tori and Meshes*
Algorithm and Application Track, Networks I, Session 2, #185

Gen-Huey Chen *An Efficient Parallel Strategy for Computing K-terminal Reliability and Finding Most Vital Edge in 2-trees and Partial 2-trees*
Algorithm and Application Track, Algorithms IV, Session 17, #353

Chi-Chang Chen *Nearly Optimal One-to-Many Parallel Routing in Star Networks*
Software Track, Networks III, Session 21, #332

Jianer Chen *Nearly Optimal One-to-Many Parallel Routing in Star Networks*
Software Track, Networks III, Session 21, #332

Andrew A. Chien *View Caching: Efficient Software Shared Memory for Dynamic Computations*
Architecture Track, Shared Memory, Session 13, #318

Jaeyoung Choi *A Fast Scalable Universal Matrix Multiplication Algorithm on Distributed-Memory Concurrent Computers*

Algorithm and Application Track, Algorithms I, Session 8, #141

Hyeong-Ah Choi *Architecture-Dependent Tuning of the Parameterized Communication Model for Optimal Multicasting*
Architecture Track, Networks II, Session 16, #290

Yungho Choi *Crossbar Analysis for Optimal Deadlock Recovery Router Architecture*
Architecture Track, Networks II, Session 16, #292

A. Choudhary *Data Access Reorganizations in Compiling Out-of-Core Data Parallel Programs on Distributed Memory Machines*
Software Track, Compilers I, Session 15, #233

Alok Choudhary *Design and Evaluation of a Data Storage and Retrieval Strategies in a Distributed Memory Continuous Media Server*
Architecture Track, I/O and Message Passing, Session 10, #274

Alok Choudhary *MTIO A Multi-Threaded Parallel I/O System*
Architecture Track, I/O and Message Passing, Session 10, #361

B. Ciciani *An Accurate Model for the Performance Analysis of Deterministic Wormhole Routing*
Software Track, Routing, Session 9, #214

Jens Clausen *Joining Forces in Solving Large-Scale Quadratic Assignment Problems in Parallel*
Algorithm and Application Track, Algorithms II, Session 11, #179

Johanne Cohen *Broadcasting and Multicasting in Cut-through Routed Networks*
Software Track, Networks III, Session 21, #339

M. Colajanni *An Accurate Model for the Performance Analysis of Deterministic Wormhole Routing*
Software Track, Routing, Session 9, #214

Alan L. Cox *Evaluating the Performance of Software Distributed Shared Memory as a Target for Parallelizing Compilers*
Architecture Track, Shared Memory, Session 13, #309

Robert Cypher *Gracefully Degradable Pipeline Networks*
Algorithm and Application Track, Networks I, Session 2, #182

D

Stefans N. Damianakis *Reducing Waiting Costs in User-Level Communication*
Architecture Track, I/O and Message Passing, Session 10, #293

Sivarama P. Danadmudi *Performance Comparison of Processor Scheduling Strategies in a Distributed-Memory Multicomputer System*
Architecture Track, Scheduling, Session 4, #129

Sajal K. Das *$O(\log \log N)$ Time Algorithms for Hamiltonian-Suffix and Min-Max-Pair Heap Operations on Hypercube Multicomputers*
Algorithm and Application Track, Algorithms III, Session 14, #208

Amitava Datta *Geometric Data Structures on a Reconfigurable Mesh, with Applications*

Algorithm and Application Track, Data Structures, Session 20, #342

Amelia De Vivo *Multiple Templates Access of Trees in Parallel Memory Systems*
Algorithm and Application Track, Data Structures, Session 20, #245

P.F.G. Dechering *Semantics and Implementation of a Generalized forall Statement for Parallel Languages*
Software Track, Compilers I, Session 15, #181

Frank Dehne *Coarse Grained Parallel Next Element Search*
Algorithm and Application Track, Algorithms I, Session 8, #128

Xiaotie Deng *A 2-D Parallel Convex Hull Algorithm with Optimal Communication Phases*
Algorithm and Application Track, Algorithms IV, Session 17, #335

M. Díaz *Logic Channels: A Coordination Approach to Distributed Programming*
Software Track, Runtime, Session 12, #213

Allen B. Downey *Predicting Queue Times on Space-sharing Parallel Computers*
Software Track, Performance Evaluation, Session 6, #203

Jose Duato *Deadlock- and Livelock-Free Routing Protocols for Wave Switching*
Architecture Track, Networks II, Session 16, #151

Cezary Dubnicki *Design and Implementation of Virtual Memory-Mapped Communication on Myrinet*
Architecture Track, I/O and Message Passing, Session 10, #330

Sandhya Dwarkadas *Evaluating the Performance of Software Distributed Shared Memory as a Target for Parallelizing Compilers*
Architecture Track, Shared Memory, Session 13, #309

Patrick Dymond *A 2-D Parallel Convex Hull Algorithm with Optimal Communication Phases*
Algorithm and Application Track, Algorithms IV, Session 17, #335

E

Guy Edjlali *Interoperability of Data Parallel Runtime Libraries*
Software Track, Runtime, Session 12, #269

K. Ekanadham *Accuracy and Speed-Up of Parallel Trace-Driven Architectural Simulation*
Architecture Track, Architecture, Session 1, #308

Richard Enbody *Comparing Gang Scheduling with Dynamic Space Sharing on Symmetric Multiprocessors Using Automatic Self-Allocating Threads (ASAT)*
Architecture Track, Synchronization and Threads, Session 7, #323

F

John D. Farrara *Performance Analysis and Optimization on a Parallel Atmospheric General Circulation Model Code*
Algorithm and Application Track, Applications, Session 5, #115

Edward W. Felten	<i>Reducing Waiting Costs in User-Level Communication</i> Architecture Track, I/O and Message Passing, Session 10, #293
Afonso Ferreira	<i>d-Dimensional Range Search on Multicomputers</i> Algorithm and Application Track, Algorithms IV, Session 17, #270
Michele Flammini	<i>Lower Bounds on Systolic Gossip</i> Algorithm and Application Track, Algorithms III, Session 14, #226
Ian Foster	<i>MTIO A Multi-Threaded Parallel I/O System</i> Architecture Track, I/O and Message Passing, Session 10, #361
Pierre Fraigniaud	<i>Broadcasting and Multicasting in Cut-through Routed Networks</i> Software Track, Networks III, Session 21, #339
Arnaud Freville	<i>A Parallel Tabu Search Algorithm for the 0-1 Multidimensional Knapsack Problem</i> Algorithm and Application Track, Algorithms III, Session 14, #218
Jason Fritts	<i>Real-Time Parallel MPEG-2 Decoding in Software</i> Algorithm and Application Track, Applications, Session 5, #219
Shiwa S. Fu	<i>Empirical Evaluation of Distributed Mutual Exclusion Algorithms</i> Architecture Track, Synchronization and Threads, Session 7, #135
Hiroaki Fujii	<i>Architecture and Performance of the Hitachi SR2201 Massively Parallel Processor System</i> Software Track, Performance Evaluation, Session 6, #383
Hiroaki Fujii	<i>Deadlock-free Fault-tolerant Routing in the Multi-dimensional Crossbar Network and its Implementation for the Hitachi SR2201</i> Software Track, Routing, Session 9, #204
Hideo Fujiwara	<i>A parallel Algorithm for Weighted Distance Transforms</i> Algorithm and Application Track, Algorithms II, Session 11, #169
Akihiro Fujiwara	<i>A parallel Algorithm for Weighted Distance Transforms</i> Algorithm and Application Track, Algorithms II, Session 11, #169
Andrea Fusiello	<i>Fault-Tolerant Deadline-Monotonic Algorithm for Scheduling Hard-Real-Time Tasks</i> Architecture Track, Scheduling, Session 4, #121

G

Guang R. Gao	<i>Latency Tolerance: A Metric for Performance Analysis of Multithreaded Architectures</i> Software Track, Performance Evaluation, Session 6, #372
Alexandros V. Gerbessiotis	<i>A Randomized Sorting Algorithm on the BSP model</i> Algorithm and Application Track, Algorithms I, Session 8, #110
Kourosh Gharachorloo	<i>Coherent Block Data Transfer in the FLASH Multiprocessor</i> Architecture Track, Architecture, Session 1, #313
A. Goldman	<i>An Efficient Parallel Algorithm for Solving the Knapsack Problem on the</i>

Hypercube
Algorithm and Application Track, Algorithms IV, Session 17, #365

K. Gopinath	<i>Alias Analysis for Fortran90 Array Slices</i> Software Track, Compilers II, Session 18, #234
Hakan Grahn	<i>Relative Performance of Hardware and Software-Only Directory Protocols Under Latency Tolerating and Reducing Techniques</i> Architecture Track, Shared Memory, Session 13, #367
Anoop Gupta	<i>Coherent Block Data Transfer in the FLASH Multiprocessor</i> Architecture Track, Architecture, Session 1, #313
Gopal Gupta	<i>Optimization Schemas for Parallel Implementation of Nondeterministic Languages and Systems</i> Software Track, Runtime, Session 12, #211
Manish Gupta	<i>On Privatization of Variables for Data-Parallel Execution</i> Software Track, Compilers I, Session 15, #167
Key Gurtzig	<i>Efficient Sorting and Routing on Reconfigurable Meshes Using Restricted Bus Length</i> Software Track, Networks III, Session 21, #232

H

Gady Haber	<i>Parallel Solutions of Indexed Recurrence Equations</i> Algorithm and Application Track, Algorithms II, Session 11, #175
Woo-Jong Hahn	<i>SPAX: A New Parallel Processing System for Commercial Application</i> Industrial Track, Invited Vendor Presentations, Session IT, #ind1
Matthew Haines	<i>Platform-Independent Runtime Optimizations Using OpenThreads</i> Software Track, Runtime, Session 12, #285
Susanne E. Hambrusch	<i>Maintaining Spatial Data Sets in Distributed-Memory Machines</i> Algorithm and Application Track, Data Structures, Session 20, #326
Sanda M. Harabagiu	<i>Parallel Inference on a Linguistic Knowledge Base</i> Algorithm and Application Track, Applications, Session 5, #288
Kenichi Harada	<i>Control Schemes in a Generalized Utility for Parallel Branch-and-Bound Algorithms</i> Algorithm and Application Track, Algorithms IV, Session 17, #366
Delbert Hart	<i>Interactive Visual Exploration of Distributed Computations</i> Software Track, Tools, Session 3, #392
Tatsuya Hayashi	<i>Work-Time Optimal k-merge Algorithms on the PRAM</i> Algorithm and Application Track, Algorithms I, Session 8, #133
Friedhelm Meyer auf der Heide	<i>Optimal Wormhole Routing in the (n,d)-Torus</i> Software Track, Routing, Session 9, #161
John Heinlein	<i>Coherent Block Data Transfer in the FLASH Multiprocessor</i> Architecture Track, Architecture, Session 1, #313

John Hennessy	<i>An Evaluation of a Commercial CC-NUMA Architecture - the CONVEX Exemplar SPP1200</i> Architecture Track, Architecture, Session 1, #304
L.O. Hertzberger	<i>An Architecture Workbench for Multicomputers</i> Software Track, Tools, Session 3, #198
Ryuichi Hirabayashi	<i>Control Schemes in a Generalized Utility for Parallel Branch-and-Bound Algorithms</i> Algorithm and Application Track, Algorithms IV, Session 17, #366
Chin-Wen Ho	<i>An Efficient Parallel Strategy for Computing K-terminal Reliability and Finding Most Vital Edge in 2-trees and Partial 2-trees</i> Algorithm and Application Track, Algorithms IV, Session 17, #353
R.Horst	<i>Maximum Delivery Time and Hot Spots in ServerNetTM Topologies</i> Industrial Track, Invited Vendor Presentations, Session IT, #ind3
Sun-Yuan Hsieh	<i>An Efficient Parallel Strategy for Computing K-terminal Reliability and Finding Most Vital Edge in 2-trees and Partial 2-trees</i> Algorithm and Application Track, Algorithms IV, Session 17, #353
Shu-Hua Hu	<i>Distributed Submesh Determination in Faulty Tori and Meshes</i> Algorithm and Application Track, Networks I, Session 2, #185
Yu Hu	<i>DPF: A Data Parallel Fortran Benchmark Suite</i> Software Track, Performance Evaluation, Session 6, #359
Rong-Yuh Hwang	<i>An Efficient Technique of Instruction Scheduling on a Superscalar-Based Multiprocessor</i> Architecture Track, Architecture, Session 1, #386
I	
Maximilian Ibel	<i>SuperWeb: Towards a Global Web-Based Parallel Computing Infrastructure</i> Software Track, Tools, Session 3, #267
Yasuhiro Inagami	<i>Architecture and Performance of the Hitachi SR2201 Massively Parallel Processor System</i> Software Track, Performance Evaluation, Session 6, #383
Yasuhiro Inagami	<i>Deadlock-free Fault-tolerant Routing in the Multi-dimensional Crossbar Network and its Implementation for the Hitachi SR2201</i> Software Track, Routing, Session 9, #204
Michiko Inoue	<i>A parallel Algorithm for Weighted Distance Transforms</i> Algorithm and Application Track, Algorithms II, Session 11, #169
Mihai F. Ionescu	<i>Optimizing Parallel Bitonic Sort</i> Algorithm and Application Track, Algorithms I, Session 8, #310
Osamu Ishihara	<i>Architecture and Performance of the Hitachi SR2201 Massively Parallel Processor System</i> Software Track, Performance Evaluation, Session 6, #383

Kazuo Iwama

Oblivious Routing Algorithms on the Mesh of Buses
Software Track, Networks III, Session 21, #317

J

Divyesh Jadav

Design and Evaluation of a Data Storage and Retrieval Strategies in a Distributed Memory Continuous Media Server
Architecture Track, I/O and Message Passing, Session 10, #274

D. Jewett

Maximum Delivery Time and Hot Spots in ServerNet™ Topologies
Industrial Track, Invited Vendor Presentations, Session IT, #ind3

Rakesh Jha

Implementation and Results of Hypothesis Testing from the C³I Parallel Benchmark Suite
Algorithm and Application Track, Applications, Session 5, #186

Susan John

An Evaluation of a Commercial CC-NUMA Architecture - the CONVEX Exemplar SPP1200
Architecture Track, Architecture, Session 1, #304

Lennart Johnsson

DPF: A Data Parallel Fortran Benchmark Suite
Software Track, Performance Evaluation, Session 6, #359

Chris R. Jones

Low Latency MPI for Meiko CS/2 and ATM Clusters
Architecture Track, I/O and Message Passing, Session 10, #206

Zoran Jovanovic

A Formal Model of Software Pipelining Loops with Conditions
Software Track, Compilers I, Session 15, #216

K

M. Kandemir

Data Access Reorganizations in Compiling Out-of-Core Data Parallel Programs on Distributed Memory Machines
Software Track, Compilers I, Session 15, #233

Vijay Karamcheti

View Caching: Efficient Software Shared Memory for Dynamic Computations
Architecture Track, Shared Memory, Session 13, #318

Mattias Karlgren

A Study of the Efficiency of Shared Attraction Memories in Cluster-Based COMA Multiprocessors
Architecture Track, Architecture, Session 1, #249

Masamori Kashiwama

Architecture and Performance of the Hitachi SR2201 Massively Parallel Processor System
Software Track, Performance Evaluation, Session 6, #383

Michael Kaufmann

Matrix Transpose on Meshes: Theory and Practice
Algorithm and Application Track, Algorithms I, Session 8, #355

Dimitris Kehagias

DPF: A Data Parallel Fortran Benchmark Suite
Software Track, Performance Evaluation, Session 6, #359

Pete Keleher

Enhancing Software DSM for Compiler-Parallelized Applications
Architecture Track, Shared Memory, Session 13, #336

Claire Kenyon	<i>d-Dimensional Range Search on Multicomputers</i> Algorithm and Application Track, Algorithms IV, Session 17, #270
Ashfaq A. Khokhar	<i>Maintaining Spatial Data Sets in Distributed-Memory Machines</i> Algorithm and Application Track, Data Structures, Session 20, #326
Soo-Won Kim	<i>SPAX: A New Parallel Processing System for Commercial Application</i> Industrial Track, Invited Vendor Presentations, Session IT, #ind1
Jonas Knopman	<i>Parallel Simulated Annealing: An Adaptive Approach</i> Algorithm and Application Track, Algorithms III, Session 14, #257
Yuetsu Kodama	<i>Experience with Fine-Grained Communication in EM-X Multiprocessor for Parallel Sparse Matrix Computation</i> Software Track, Performance Evaluation, Session 6, #319
Makoto Koga	<i>Architecture and Performance of the Hitachi SR2201 Massively Parallel Processor System</i> Software Track, Performance Evaluation, Session 6, #383
Jean-Claude Konig	<i>Broadcasting and Multicasting in Cut-through Routed Networks</i> Software Track, Networks III, Session 21, #339
Nectarios Koziris	<i>Optimal Scheduling for UET-UCT Generalized n-Dimensional Grid Task Graphs</i> Architecture Track, Scheduling, Session 4, #162
Eileen Kraemer	<i>Causality Filters: A Tool for the Online Visualization and Steering of Parallel and Distributed Programs</i> Software Track, Tools, Session 3, #340
Eileen Kraemer	<i>Interactive Visual Exploration of Distributed Computations</i> Software Track, Tools, Session 3, #392
F. Kuijman	<i>Semantics and Implementation of a Generalized forall Statement for Parallel Languages</i> Software Track, Compilers I, Session 15, #181
Manfred Kunde	<i>Efficient Sorting and Routing on Reconfigurable Meshes Using Restricted Bus Length</i> Software Track, Networks III, Session 21, #232

L

Jesus Labarta	<i>Analysis of Several Scheduling Algorithms under the Nano-Threads Programming Model</i> Architecture Track, Synchronization and Threads, Session 7, #217
Ambrose K. Laing	<i>Gracefully Degradable Pipeline Networks</i> Algorithm and Application Track, Networks I, Session 2, #182
Anders Landin	<i>A Study of the Efficiency of Shared Attraction Memories in Cluster-Based COMA Multiprocessors</i> Architecture Track, Architecture, Session 1, #249

Koen Langendoen	<i>Platform-Independent Runtime Optimizations Using OpenThreads</i> Software Track, Runtime, Session 12, #285
Thomas Lengauer	<i>Parallel 'Go with the Winners' Algorithms in the LogP Model</i> Architecture Track, Architecture Theory, Session 19, #375
Michael Lenke	<i>A Tool for On-Line Visualization and Interactive Steering of Parallel HPC Applications</i> Algorithm and Application Track, Applications, Session 5, #177
Kai Li	<i>Design and Implementation of Virtual Memory-Mapped Communication on Myrinet</i> Architecture Track, I/O and Message Passing, Session 10, #330
Zhiyuan Li	<i>Empirical Evaluation of Distributed Mutual Exclusion Algorithms</i> Architecture Track, Synchronization and Threads, Session 7, #135
Hock-Beng Lim	<i>A Compiler-Directed Cache Coherence Scheme Using Data Prefetching</i> Software Track, Compilers II, Session 18, #341
Jing-Chiou Liou	<i>A Comparison of General Approaches to Multiprocessor Scheduling</i> Architecture Track, Scheduling, Session 4, #209
Jyh-Charn Liu	<i>A Hybrid Interconnection Network for Integrated Communication Services</i> Software Track, Routing, Session 9, #278
Peter S. Lomdahl	<i>Extensible Message Passing Application Development and Debugging with Python</i> Software Track, Compilers II, Session 18, #251
Pedro López	<i>Deadlock- and Livelock-Free Routing Protocols for Wave Switching</i> Architecture Track, Networks II, Session 16, #151
John Z. Lou	<i>Performance Analysis and Optimization on a Parallel Atmospheric General Circulation Model Code</i> Algorithm and Application Track, Applications, Session 5, #115
Paul Lu	<i>Aurora: Scoped Behavior for Per-Context Optimized Distributed Data Sharing</i> Architecture Track, Shared Memory, Session 13, #277
Honghui Lu	<i>Evaluating the Performance of Software Distributed Shared Memory as a Target for Parallelizing Compilers</i> Architecture Track, Shared Memory, Session 13, #309

M

Shikharesh Majumdar	<i>Performance Comparison of Processor Scheduling Strategies in a Distributed-Memory Multicomputer System</i> Architecture Track, Scheduling, Session 4, #129
Luigi Mancini	<i>Fault-Tolerant Deadline-Monotonic Algorithm for Scheduling Hard-Real-Time Tasks</i> Architecture Track, Scheduling, Session 4, #121

Jeff Marquis	<i>DFRN: A New Approach on Duplication Based Scheduling for Distributed Memory Multiprocessor Systems</i> Architecture Track, Scheduling, Session 4, #212
Xavier Martorell	<i>Analysis of Several Scheduling Algorithms under the Nano-Threads Programming Model</i> Architecture Track, Synchronization and Threads, Session 7, #217
Ambros Marzetta	<i>Joining Forces in Solving Large-Scale Quadratic Assignment Problems in Parallel</i> Algorithm and Application Track, Algorithms II, Session 11, #179
Toshimitsu Masuzawa	<i>A parallel Algorithm for Weighted Distance Transforms</i> Algorithm and Application Track, Algorithms II, Session 11, #169
Marios Mavronicolas	<i>The Impact of Timing on Linearizability in Counting Networks</i> Algorithm and Application Track, Data Structures, Session 20, #150
R. Melhem	<i>Modeling Communication Costs in Multiplexed Optical Switching Networks</i> Algorithm and Application Track, Networks I, Session 2, #237
Ulrich Meyer	<i>Matrix Transpose on Meshes: Theory and Practice</i> Algorithm and Application Track, Algorithms I, Session 8, #355
M. Michael	<i>Accuracy and Speed-Up of Parallel Trace-Driven Architectural Simulation</i> Architecture Track, Architecture, Session 1, #308
Maged M. Michael	<i>Relative Performance of Preemption-Safe Locking and Non-Blocking Synchronization on Multiprogrammed Shared Memory Multiprocessors</i> Architecture Track, Synchronization and Threads, Session 7, #300
Dragan Milicev	<i>A Formal Model of Software Pipelining Loops with Conditions</i> Software Track, Compilers I, Session 15, #216
Eiji Miyano	<i>Oblivious Routing Algorithms on the Mesh of Buses</i> Software Track, Networks III, Session 21, #317
Dan I. Moldovan	<i>Parallel Inference on a Linguistic Knowledge Base</i> Algorithm and Application Track, Applications, Session 5, #288
Lantz Moore	<i>External Adjustment of Runtime Parameters in Time Warp Synchronized Parallel Simulators</i> Architecture Track, Synchronization and Threads, Session 7, #138
Sachin More	<i>MTIO A Multi-Threaded Parallel I/O System</i> Architecture Track, I/O and Message Passing, Session 10, #361
Vasily G. Moshnyaga	<i>A Memory Efficient Array Architecture for Real-Time Motion Estimation</i> Architecture Track, Architecture, Session 1, #373
Silvia M. Mueller	<i>Conflict-Free Access to Multiple Single-Ported Register Files</i> Architecture Track, Architecture Theory, Session 19, #127
Mustafa Muhamad	<i>Implementation and Results of Hypothesis Testing from the C^3I Parallel</i>

N

Junji Nakagoshi	<i>Deadlock-free Fault-tolerant Routing in the Multi-dimensional Crossbar Network and its Implementation for the Hitachi SR2201</i> Software Track, Routing, Session 9, #204
Koji Nakano	<i>Work-Time Optimal k-merge Algorithms on the PRAM</i> Algorithm and Application Track, Algorithms I, Session 8, #133
A. Nanda	<i>Accuracy and Speed-Up of Parallel Trace-Driven Architectural Simulation</i> Architecture Track, Architecture, Session 1, #308
Nacho Navarro	<i>Analysis of Several Scheduling Algorithms under the Nano-Threads Programming Model</i> Architecture Track, Synchronization and Threads, Session 7, #217
Shashank S. Nemawarkar	<i>Latency Tolerance: A Metric for Performance Analysis of Multithreaded Architectures</i> Software Track, Performance Evaluation, Session 6, #372
A-T. Nguyen	<i>Accuracy and Speed-Up of Parallel Trace-Driven Architectural Simulation</i> Architecture Track, Architecture, Session 1, #308
Lionel M. Ni	<i>Architecture-Dependent Tuning of the Parameterized Communication Model for Optimal Multicasting</i> Architecture Track, Networks II, Session 16, #290
Smail Niar	<i>A Parallel Tabu Search Algorithm for the 0-1 Multidimensional Knapsack Problem</i> Algorithm and Application Track, Algorithms III, Session 14, #218
Natawut Nupairoj	<i>Architecture-Dependent Tuning of the Parameterized Communication Model for Optimal Multicasting</i> Architecture Track, Networks II, Session 16, #290

O

Stephan Olariu	<i>Work-Time Optimal k-merge Algorithms on the PRAM</i> Algorithm and Application Track, Algorithms I, Session 8, #133
Stephan Olariu	<i>On the Dynamic Initialization of Parallel Computers</i> Architecture Track, Architecture Theory, Session 19, #157
K. Omang	<i>Scalability of SCI Workstation Clusters: A Preliminary Study</i> Industrial Track, Invited Vendor Presentations, Session IT, #ind2

P

Michael A. Palis	<i>A Comparison of General Approaches to Multiprocessor Scheduling</i> Architecture Track, Scheduling, Session 4, #209
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Dhabaleswar K. Panda	<i>A Reliable Hardware Barrier Synchronization Schemes</i> Architecture Track, Synchronization and Threads, Session 7, #322
C. Paolucci	<i>An Accurate Model for the Performance Analysis of Deterministic Wormhole Routing</i> Software Track, Routing, Session 9, #214
George Papakonstantinou	<i>Optimal Scheduling for UET-UCT Generalized n-Dimensional Grid Task Graphs</i> Architecture Track, Scheduling, Session 4, #162
Marina Paptriantafilou	<i>The Impact of Timing on Linearizability in Counting Networks</i> Algorithm and Application Track, Data Structures, Session 20, #150
B. Parady	<i>Scalability of SCI Workstation Clusters: A Preliminary Study</i> Industrial Track, Invited Vendor Presentations, Session IT, #ind2
Behrooz Parhami	<i>Cyclic Networks: A Family of Versatile Fixed-Degree Interconnection Architectures</i> Software Track, Networks III, Session 21, #387
Ju-Young L. Park	<i>Architecture-Dependent Tuning of the Parameterized Communication Model for Optimal Multicasting</i> Architecture Track, Networks II, Session 16, #290
Gyung-Leen Park	<i>DFRN: A New Approach on Duplication Based Scheduling for Distributed Memory Multiprocessor Systems</i> Architecture Track, Scheduling, Session 4, #212
Marcus Peinado	<i>Parallel 'Go with the Winners' Algorithms in the LogP Model</i> Architecture Track, Architecture Theory, Session 19, #375
Stephane Pérennès	<i>Lower Bounds on Systolic Gossip</i> Algorithm and Application Track, Algorithms III, Session 14, #226
Michael Perregaard	<i>Joining Forces in Solving Large-Scale Quadratic Assignment Problems in Parallel</i> Algorithm and Application Track, Algorithms II, Session 11, #179
Fabrizio Petrini	<i>k-ary n-trees: High Performance Networks for Massively Parallel Architectures</i> Algorithm and Application Track, Networks I, Session 2, #299
Fabrizio Petrini	<i>Performance Analysis of Minimal Adaptive Wormhole Routing with Time-Dependent Deadlock Recovery</i> Architecture Track, Networks II, Session 16, #298
Jim F. Philbin	<i>Design and Implementation of Virtual Memory-Mapped Communication on Myrinet</i> Architecture Track, I/O and Message Passing, Session 10, #330
A.D. Pimentel	<i>An Architecture Workbench for Multicomputers</i> Software Track, Tools, Session 3, #198
Timothy Mark Pinkston	<i>Crossbar Analysis for Optimal Deadlock Recovery Router Architecture</i> Architecture Track, Networks II, Session 16, #292

Timothy Mark Pinkston	<i>Characterization of Deadlocks in Interconnection Networks</i> Algorithm and Application Track, Networks I, Session 2, #291
M. Cristina Pinotti	<i>O(log log N) Time Algorithms for Hamiltonian-Suffix and Min-Max-Pair Heap Operations on Hypercube Multicomputers</i> Algorithm and Application Track, Algorithms III, Session 14, #208
Luiz Pires	<i>Implementation and Results of Hypothesis Testing from the C³I Parallel Benchmark Suite</i> Algorithm and Application Track, Applications, Session 5, #186
Enrico Pontelli	<i>Optimization Schemas for Parallel Implementation of Nondeterministic Languages and Systems</i> Software Track, Runtime, Session 12, #211
Athanassios Poulakidas	<i>Dynamic Processor Scheduling with Client Resources for Fast Multi-resolution WWW Image Browsing</i> Architecture Track, Scheduling, Session 4, #327
R	
Radharamanan Radhakrishnan	<i>External Adjustment of Runtime Parameters in Time Warp Synchronized Parallel Simulators</i> Architecture Track, Synchronization and Threads, Session 7, #138
Sanguthevar Rajasekaran	<i>Designing Efficient Distributed Algorithms Using Sampling Techniques</i> Algorithm and Application Track, Algorithms II, Session 11, #136
Andre Raspaud	<i>Broadcasting and Multicasting in Cut-through Routed Networks</i> Software Track, Networks III, Session 21, #339
Sabine Rathmayer	<i>A Tool for On-Line Visualization and Interactive Steering of Parallel HPC Applications</i> Algorithm and Application Track, Applications, Session 5, #177
Andrew Rau-Chaplin	<i>d-Dimensional Range Search on Multicomputers</i> Algorithm and Application Track, Algorithms IV, Session 17, #270
Andrew Rau-Chaplin	<i>Coarse Grained Parallel Next Element Search</i> Algorithm and Application Track, Algorithms I, Session 8, #128
Kee-Wook Rim	<i>SPAX: A New Parallel Processing System for Commercial Application</i> Industrial Track, Invited Vendor Presentations, Session IT, #ind1
Gruia-Catalin Roman	<i>Interactive Visual Exploration of Distributed Computations</i> Software Track, Tools, Session 3, #392
Mendel Rosenblum	<i>Coherent Block Data Transfer in the FLASH Multiprocessor</i> Architecture Track, Architecture, Session 1, #313
Sumit Roy	<i>A Comparison of Parallel Approaches for Algebraic Factorization in Logic Synthesis</i> Architecture Track, Architecture Theory, Session 19, #394
B. Rubio	<i>Logic Channels: A Coordination Approach to Distributed Programming</i> Software Track, Runtime, Session 12, #213

S

Shuichi Sakai	<i>Experience with Fine-Graine Communication in EM-X Multiprocessor for Parallel Sparse Matrix Computation</i> Software Track, Performance Evaluation, Session 6, #319
Hirofumi Sakane	<i>Experience with Fine-Graine Communication in EM-X Multiprocessor for Parallel Sparse Matrix Computation</i> Software Track, Performance Evaluation, Session 6, #319
Rizos Sakellariou	<i>A Compile-Time Partitioning Strategy for Non-Rectangular Loop Nests</i> Software Track, Compilers II, Session 18, #268
C. Salisbury	<i>Modeling Communication Costs in Multiplexed Optical Switching Networks</i> Algorithm and Application Track, Networks I, Session 2, #237
Joel Saltz	<i>Interoperability of Data Parallel Runtime Libraries</i> Software Track, Runtime, Session 12, #269
Joel Saltz	<i>A Customizable Simulator for Workstation Networks</i> Software Track, Performance Evaluation, Session 6, #337
Mitsuhisa Sato	<i>Experience with Fine-Graine Communication in EM-X Multiprocessor for Parallel Sparse Matrix Computation</i> Software Track, Performance Evaluation, Session 6, #319
Vittorio Scarano	<i>Multiple Templates Access of Trees in Parallel Memory Systems</i> Algorithm and Application Track, Data Structures, Session 20, #245
Klaus E. Schauser	<i>Optimizing Parallel Bitonic Sort</i> Algorithm and Application Track, Algorithms I, Session 8, #310
Klaus E. Schauser	<i>SuperWeb: Towards a Global Web-Based Parallel Computing Infrastructure</i> Software Track, Tools, Session 3, #267
Christian Scheideler	<i>Optimal Wormhole Routing in the (n,d)-Torus</i> Software Track, Routing, Session 9, #161
Chris J. Scheiman	<i>SuperWeb: Towards a Global Web-Based Parallel Computing Infrastructure</i> Software Track, Tools, Session 3, #267
Karsten Schwan	<i>High Performance Computational Steering of Physical Simulations</i> Software Track, Tools, Session 3, #396
Michael L. Scott	<i>Relative Performance of Preemption-Safe Locking and Non-Blocking Synchronization on Multiprogrammed Shared Memory Multiprocessors</i> Architecture Track, Synchronization and Threads, Session 7, #300
R. Seshadri	<i>Alias Analysis for Fortran90 Array Slices</i> Software Track, Compilers II, Session 18, #234
Charles Severance	<i>Comparing Gang Scheduling with Dynamic Space Sharing on Symmetric Multiprocessors Using Automatic Self-Allocating Threads</i>

(ASAT)
Architecture Track, Synchronization and Threads, Session 7, #323

Nadia Shalaby	<i>DPF: A Data Parallel Fortran Benchmark Suite</i> Software Track, Performance Evaluation, Session 6, #359
Jau-Der Shih	<i>Adaptive Fault-Tolerant Wormhole Routing Algorithms for Hypercube and Mesh Interconnection Networks</i> Software Track, Routing, Session 9, #194
Yuji Shinano	<i>Control Schemes in a Generalized Utility for Parallel Branch-and-Bound Algorithms</i> Algorithm and Application Track, Algorithms IV, Session 17, #366
Behrooz Shirazi	<i>DFRN: A New Approach on Duplication Based Scheduling for Distributed Memory Multiprocessor Systems</i> Architecture Track, Scheduling, Session 4, #212
V. Shurbanov	<i>Maximum Delivery Time and Hot Spots in ServerNet™ Topologies</i> Industrial Track, Invited Vendor Presentations, Session IT, #ind3
Jop Sibeyn	<i>Matrix Transpose on Meshes: Theory and Practice</i> Algorithm and Application Track, Algorithms I, Session 8, #355
Jaswinder Pal Singh	<i>Real-Time Parallel MPEG-2 Decoding in Software</i> Algorithm and Application Track, Applications, Session 5, #219
Amit Pal Singh	<i>An Evaluation of a Commercial CC-NUMA Architecture - the CONVEX Exemplar SPP1200</i> Architecture Track, Architecture, Session 1, #304
Ambuj K. Singh	<i>Low Latency MPI for Meiko CS/2 and ATM Clusters</i> Architecture Track, I/O and Message Passing, Session 10, #206
Jaswinder Pal Singh	<i>An Evaluation of a Commercial CC-NUMA Architecture - the CONVEX Exemplar SPP1200</i> Architecture Track, Architecture, Session 1, #304
Constantinos J. Siniolakis	<i>A Randomized Sorting Algorithm on the BSP model</i> Algorithm and Application Track, Algorithms I, Session 8, #110
H.J. Sips	<i>Semantics and Implementation of a Generalized forall Statement for Parallel Languages</i> Software Track, Compilers I, Session 15, #181
Rajeev Sivaram	<i>A Reliable Hardware Barrier Synchronization Schemes</i> Architecture Track, Synchronization and Threads, Session 7, #322
Robert Snelick	<i>S-Check: A Tool for Tuning Parallel Programs</i> Software Track, Tools, Session 3, #282
Chutimet Srinilta	<i>Design and Evaluation of a Data Storage and Retrieval Strategies in a Distributed Memory Continuous Media Server</i> Architecture Track, I/O and Message Passing, Session 10, #274
Per Stenström	<i>Relative Performance of Hardware and Software-Only Directory Protocols Under Latency Tolerating and Reducing Techniques</i>

Architecture Track, Shared Memory, Session 13, #367

Ivan Stojmenovic

On the Dynamic Initialization of Parallel Computers
Architecture Track, Architecture Theory, Session 19, #157

Craig B. Stunkel

A Reliable Hardware Barrier Synchronization Schemes
Architecture Track, Synchronization and Threads, Session 7, #322

Tsutomu Sumimoto

Deadlock-free Fault-tolerant Routing in the Multi-dimensional Crossbar Network and its Implementation for the Hitachi SR2201
Software Track, Routing, Session 9, #204

Tsutomu Sumimoto

Architecture and Performance of the Hitachi SR2201 Massively Parallel Processor System
Software Track, Performance Evaluation, Session 6, #383

Yuzhong Sun

Hybrid Time Synchronization Implemented Through Special Ring Array for Mesh or Torus
Architecture Track, Networks II, Session 16, #116

Alan Sussman

Interoperability of Data Parallel Runtime Libraries
Software Track, Runtime, Session 12, #269

Willy Swaenepoel

Evaluating the Performance of Software Distributed Shared Memory as a Target for Parallelizing Compilers
Architecture Track, Shared Memory, Session 13, #309

T

Keikichi Tamaru

A Memory Efficient Array Architecture for Real-Time Motion Estimation
Architecture Track, Architecture, Session 1, #373

Teruo Tanaka

Deadlock-free Fault-tolerant Routing in the Multi-dimensional Crossbar Network and its Implementation for the Hitachi SR2201
Software Track, Routing, Session 9, #204

Radhika Thekkath

An Evaluation of a Commercial CC-NUMA Architecture - the CONVEX Exemplar SPP1200
Architecture Track, Architecture, Session 1, #304

Jesper Larsson Träff

A Parallel Priority Data Structure with Applications
Algorithm and Application Track, Data Structures, Session 20, #174

Maria A. Trenas

The Sparse Cyclic Distribution against its Dense Counterparts
Software Track, Compilers II, Session 18, #302

J.M. Troya

Logic Channels: A Coordination Approach to Distributed Programming
Software Track, Runtime, Session 12, #213

D. Trystram

An Efficient Parallel Algorithm for Solving the Knapsack Problem on the Hypercube
Algorithm and Application Track, Algorithms IV, Session 17, #365

Panayotis Tsanakas

Optimal Scheduling for UET-UCT Generalized n-Dimensional Grid Task Graphs
Architecture Track, Scheduling, Session 4, #162

Chau-Wen Tseng	<i>Enhancing Software DSM for Compiler-Parallelized Applications</i> Architecture Track, Shared Memory, Session 13, #336
Philippas Tsigas	<i>The Impact of Timing on Linearizability in Counting Networks</i> Algorithm and Application Track, Data Structures, Session 20, #150
Nian-Feng Tzeng	<i>Empirical Evaluation of Distributed Mutual Exclusion Algorithms</i> Architecture Track, Synchronization and Threads, Session 7, #135

U

Stephane Ubéda	<i>d-Dimensional Range Search on Multicomputers</i> Algorithm and Application Track, Algorithms IV, Session 17, #270
Manuel Ujaldon	<i>The Sparse Cyclic Distribution against its Dense Counterparts</i> Software Track, Compilers II, Session 18, #302
Mustafa Uysal	<i>A Customizable Simulator for Workstation Networks</i> Software Track, Performance Evaluation, Session 6, #337

V

C. van Reeuwijk	<i>Semantics and Implementation of a Generalized forall Statement for Parallel Languages</i> Software Track, Compilers I, Session 15, #181
Marco Vanneschi	<i>Performance Analysis of Minimal Adaptive Wormhole Routing with Time-Dependent Deadlock Recovery</i> Architecture Track, Networks II, Session 16, #298
Brian VanVoorst	<i>Implementation and Results of Hypothesis Testing from the C³I Parallel Benchmark Suite</i> Algorithm and Application Track, Applications, Session 5, #186
Jeffrey Vetter	<i>High Performance Computational Steering of Physical Simulations</i> Software Track, Tools, Session 3, #396
Uzi Vishkin	<i>Conflict-Free Access to Multiple Single-Ported Register Files</i> Architecture Track, Architecture Theory, Session 19, #127

W

Hideo Wada	<i>Deadlock-free Fault-tolerant Routing in the Multi-dimensional Crossbar Network and its Implementation for the Hitachi SR2201</i> Software Track, Routing, Session 9, #204
Hideo Wada	<i>Architecture and Performance of the Hitachi SR2201 Massively Parallel Processor System</i> Software Track, Performance Evaluation, Session 6, #383
Jianchao Wang	<i>Wide-Sense Nonblocking Clos Networks under Packing Strategy</i> Algorithm and Application Track, Networks I, Session 2, #112
Sugath Warnakulasuriya	<i>Characterization of Deadlocks in Interconnection Networks</i> Algorithm and Application Track, Networks I, Session 2, #291

W. Watson	<i>Maximum Delivery Time and Hot Spots in ServerNet™ Topologies</i> Industrial Track, Invited Vendor Presentations, Session IT, #ind3
David Watson	<i>Dynamic Processor Scheduling with Client Resources for Fast Multi-resolution WWW Image Browsing</i> Architecture Track, Scheduling, Session 4, #327
David S.L. Wei	<i>Designing Efficient Distributed Algorithms Using Sampling Techniques</i> Algorithm and Application Track, Algorithms II, Session 11, #136
Philip A. Wilsey	<i>External Adjustment of Runtime Parameters in Time Warp Synchronized Parallel Simulators</i> Architecture Track, Synchronization and Threads, Session 7, #138
Patrick Worley	<i>Performance Prediction for Complex Parallel Applications</i> Algorithm and Application Track, Applications, Session 5, #178
X	
Zhaoyun Xing	<i>Parallel Global Routing Algorithms for Standard Cells</i> Algorithm and Application Track, Algorithms III, Session 14, #284
Zhiwei Xu	<i>Hybrid Time Synchronization Implemented Through Special Ring Array for Mesh or Torus</i> Architecture Track, Networks II, Session 16, #116
Ming Q. Xu	<i>MTIO A Multi-Threaded Parallel I/O System</i> Architecture Track, I/O and Message Passing, Session 10, #361
Chengzhong Xu	<i>Time-Stamping Algorithms for Parallelization of Loops at Run-Time</i> Software Track, Runtime, Session 12, #223
Y	
Sudhakar Yalamanchili	<i>Deadlock- and Livelock-Free Routing Protocols for Wave Switching</i> Architecture Track, Networks II, Session 16, #151
Yoshinori Yamaguchi	<i>Experience with Fine-Grained Communication in EM-X Multiprocessor for Parallel Sparse Matrix Computation</i> Software Track, Performance Evaluation, Session 6, #319
Hayato Yamana	<i>Experience with Fine-Grained Communication in EM-X Multiprocessor for Parallel Sparse Matrix Computation</i> Software Track, Performance Evaluation, Session 6, #319
Tao Yang	<i>Dynamic Processor Scheduling with Client Resources for Fast Multi-resolution WWW Image Browsing</i> Architecture Track, Scheduling, Session 4, #327
Yuanyuan Yang	<i>Wide-Sense Nonblocking Clos Networks under Packing Strategy</i> Algorithm and Application Track, Networks I, Session 2, #112
Yoshiko Yasuda	<i>Deadlock-free Fault-tolerant Routing in the Multi-dimensional Crossbar Network and its Implementation for the Hitachi SR2201</i> Software Track, Routing, Session 9, #204

Yoshiko Yasuda	<i>Architecture and Performance of the Hitachi SR2201 Massively Parallel Processor System</i> Software Track, Performance Evaluation, Session 6, #383
Chi-Hsiang Yeh	<i>Cyclic Networks: A Family of Versatile Fixed-Degree Interconnection Architectures</i> Software Track, Networks III, Session 21, #387
Pen-Chung Yew	<i>A Compiler-Directed Cache Coherence Scheme Using Data Prefetching</i> Software Track, Compilers II, Session 18, #341
L.Young	<i>Maximum Delivery Time and Hot Spots in ServerNetTM Topologies</i> Industrial Track, Invited Vendor Presentations, Session IT, #ind3
Z	
Emilio L. Zapata	<i>The Sparse Cyclic Distribution against its Dense Counterparts</i> Software Track, Compilers II, Session 18, #302
Christos D. Zaroliagis	<i>A Parallel Priority Data Structure with Applications</i> Algorithm and Application Track, Data Structures, Session 20, #174
Jieliang Zhou	<i>A 2-D Parallel Convex Hull Algorithm with Optimal Communication Phases</i> Algorithm and Application Track, Algorithms IV, Session 17, #335
Mingfa Zhu	<i>Hybrid Time Synchronization Implemented Through Special Ring Array for Mesh or Torus</i> Architecture Track, Networks II, Session 16, #116
Eugene V. Zima	<i>Fast Parallel Computation of the Polynomial Shift</i> Algorithm and Application Track, Algorithms II, Session 11, #165
Albert Y. Zomaya	<i>On the Dynamic Initialization of Parallel Computers</i> Architecture Track, Architecture Theory, Session 19, #157